THE DESIGN OF DIGITAL SIGNAL PROCESSING ELECTRONICS FOR A STEEL WIRE ROPETESTING INSTRUMENT

by

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DISSERTATION

presented in completion for

MASTERS DIPLOMA
in
TECHNOLOGY
in
ELECTRICAL ENGINEERING

in the

FACULTY OF ENGINEERING

at the

M L SULTAN TECHNIKON

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NOVEMBER 1989

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SYNOPSIS

This thesis describes the design work undertaken at the Anglo American Electronics Laboratory to implement an electronic instrumentation system to evaluate the condition of steel wire ropes.

The instrument design is a spin off from the successful development of a magnetic test head that can detect area, contact and broken wires effectively and independently of each other. Therefore all three parameters can be measured simultaneously with a single instrument. At present no other instrument can do this. The test head design is described in a thesis entitled " Die Electromagnetiese Toetsing van Staaltoue met behulp van Permanente Magnete ".

The processing methods that are to be used on the prototype instrument are described. The system design places particular emphasis on instrument intelligence, an easy to use operator interface and the ability to run complex mathematical routines in real time.

The main body of this thesis consists of the design of the electronics. The signals from the test head are low level analog signals. The precautions taken to ensure signal integrity are described in Chapter 4 and Chapter 11. Both analog and digital timing are crucial to the instrument

design and reliability. A detailed description of the timing is presented for each device interfaced.

ACKNOWLEDGEMENTS

This work was born out of the need for a composite steel wire rope testing instrument at the Anglo American Rope Testing division. In particular great debt is owed to Dr N T van der Walt for his work on the successful development of the test head. He has made numerous suggestions concerning the electronics throughout the project.

I am grateful to B G Shereston and D J Bailey for their influence and encouragement during the project. As a result of their pioneering work on the TMS32010 digital signal processing system the need arose for a more powerful system.

Appreciation is also expressed to Mr B Govind, Miss N B Naidoo, Mr S Nair and Dr R W Scott for providing assistance during the final stages of the manuscript. Their criticisms were most helpful.

I thank the Management of the Anglo American Electronics Laboratory for allowing this project to be presented as a dissertation at the M L Sultan Technikon.

CHAPTER 1

1.0 INTRODUCTION

Steel wire ropes are used extensively in the mining industry. These ropes are constructed by combining many single strands of steel wires. After prolonged use the condition of the rope deteriorates because of corrosion and fatigue. Corrosion causes loss in metal area of the rope. Physical stresses cause change in interwire contact and broken wires. These defects reduce the strength of the rope and in time the reliability of the rope becomes questionable. There are two methods that are used to evaluate the condition of the rope; visual and electronic non-destructive testing.

1.1 Visual Inspection

To assess rope condition use is made of accessible visual data on rope deterioration indices. The strength of the rope is therefore only dependent on the relationship between reduction of rope strength and the visual condition on the surface. This is not a very suitable method for the inspection of the rope because not all the deterioration indices are visible. Such systematic inspections by skilled and experienced engineers render only fair approximation of the factor of safety. Another disadvantage of this method is that results may not always be consistent because of the human factor involved. This situation is changed markedly by the use of magnetic non-destructive rope inspection.

1.2 Magnetic Non-Destructive Inspection

AC and DC magnetic methods of inspection have been implemented. The AC instrument magnetises the rope using an alternating current. Sensors are used to pick up the loss of metallic area, and change in interwire contact. The DC instrument uses a permanent magnetic field. Broken wires are detected using the DC instrument. A printout of the defects is produced and these results are evaluated. Visual inspection may be carried out in certain suspect areas. It is obvious then that in order for a rope to be tested for broken wires, loss in metallic area and change in interwire contact at least two tests have to be performed on the same rope. This results in greater testing time and hence loss in production. The AC instrument is difficult to use and thicker ropes require a more powerful instrument. It was out of this that a need for a single instrument to measure all three modes of deterioration arose at the Anglo American Corporation. The advantages to be gained by such an instrument are shorter testing time, an increase in productivity and a more cost effective instrument.

1.3 Anglo American Electronic Laboratory's (AAEL) Involvement

AAEL has an established involvement in steel wire rope testing instrumentation. Their research and development span more than twenty years. Two instruments were developed and refined at the laboratory. These are the AC380 and DC313 instruments. Both of these instruments have performed very satisfactorily and they are virtual standards among the rope testing industry in Southern

Africa. International patents have been awarded for both these instruments. Plate 1 shows the AAEL Rope Test Facility.

1.4 New Steel Wire Rope Tester Development

Figure 1 shows the block diagram of the rope tester.The magnetic testhead development has been completed by Dr. N.T. van der Walt (Die Elektromagnetiese Toetsing van Staaltoue met behulp van Permanente Magnete). Three signals are available for processing, loss in metallic area, broken wires and interwire contact. The area and contact signals require integration and the broken wire signals require other processing. Plate 2 shows the test head on the rope.

1.5 Analog Integrators

Analog integrators were the first logical choice in this project. After designing these integrators with op-amps with ultra low offsets, it became apparent that the electronics for this instrument would present serious problems. Every single source of voltage would need to be evaluated in the critical paths in the integrator. The integrators need a maximum gain of one hundred. At this gain an offset voltage of a few microvolts when integrated over a period of time becomes appreciable. One needs to consider that a typical test run takes twenty minutes. Drift in analog integrators can be misintepreted as an anamoly in the rope. For this reason it was decided to investigate digital signal processing.

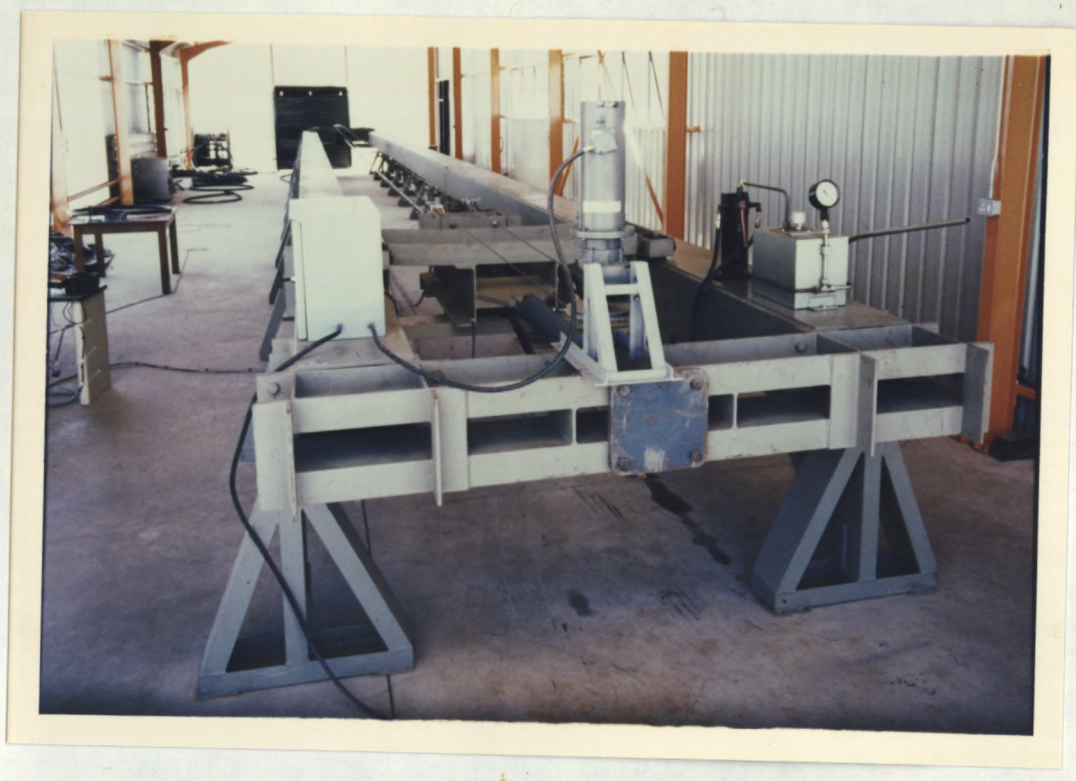


PLATE 1

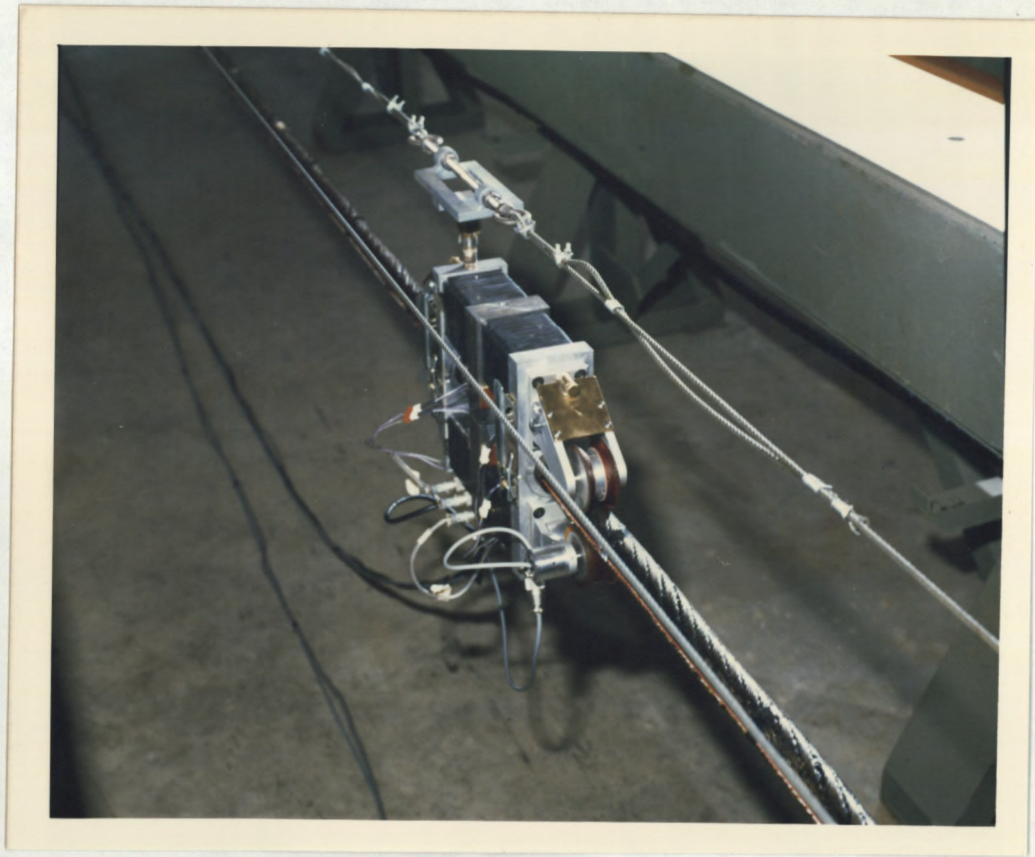


PLATE 2

1.6 Digital Integrators

Software offers great flexibilty in instrument design. Offsets can be evaluated every few milliseconds and compensated for. Digital integrators have excellent noise immunity. By selecting components with good temperature coefficients, the instrument should perform satisfactorily over a wide temperature range. Area deviations can be measured in software and printed on the chart recorder, obviating the need for the operator to perform repeated calculations. Broken wires can be sifted out of signals generated by corrosion using template comparision techniques. These are then counted providing a total broken wire count at the end of the run. Digital filtering of rope noise can be implemented. The disadvantages of the digital system are greater costs and increased complexity. It can be readily seen that digital processing offers numerous advantages not easily implemented in analog.

1.7 The Proposed System Electronics

An evaluation system was built around the TMS32010 digital signal processor. These circuit boards were designed for the AAEL fire detection system. With only slight modifications and a software change three of these boards were used to process the signals of interest in order to demonstrate the feasibilty of the system.

Evaluation tests performed with the instrument produced satisfactory traces of rope anomalies and also revealed shortcomings of the instrument. These are listed below:

1. Excessive power consumption of the DSP circuits. The 5V circuits consumed 9 amperes. This is far from the ideal required for a portable instrument expected to offer testing time of 6 hours. Using Nicad batteries the current consumption has to be below 1 ampere to meet the testing time requirement of 6 hours.

2. Limited processing speed of the TMS32010.

To overcome the above problems the TMS320C25 processor was chosen. It offers an enhanced instruction set, and its processing speed is 12 million floating point operations per second. CMOS fabrication ensures extremely low power consumption.

A block diagram of the proposed system is shown in Figure 1. The functions of each block are listed below.

Magnetic Test Head: Pick-up of the change in the magnetic properties caused by mechanical defects in the steel wire rope.

Digital Signal Processor System : Perform real time digital signal processing on each of the input signals.

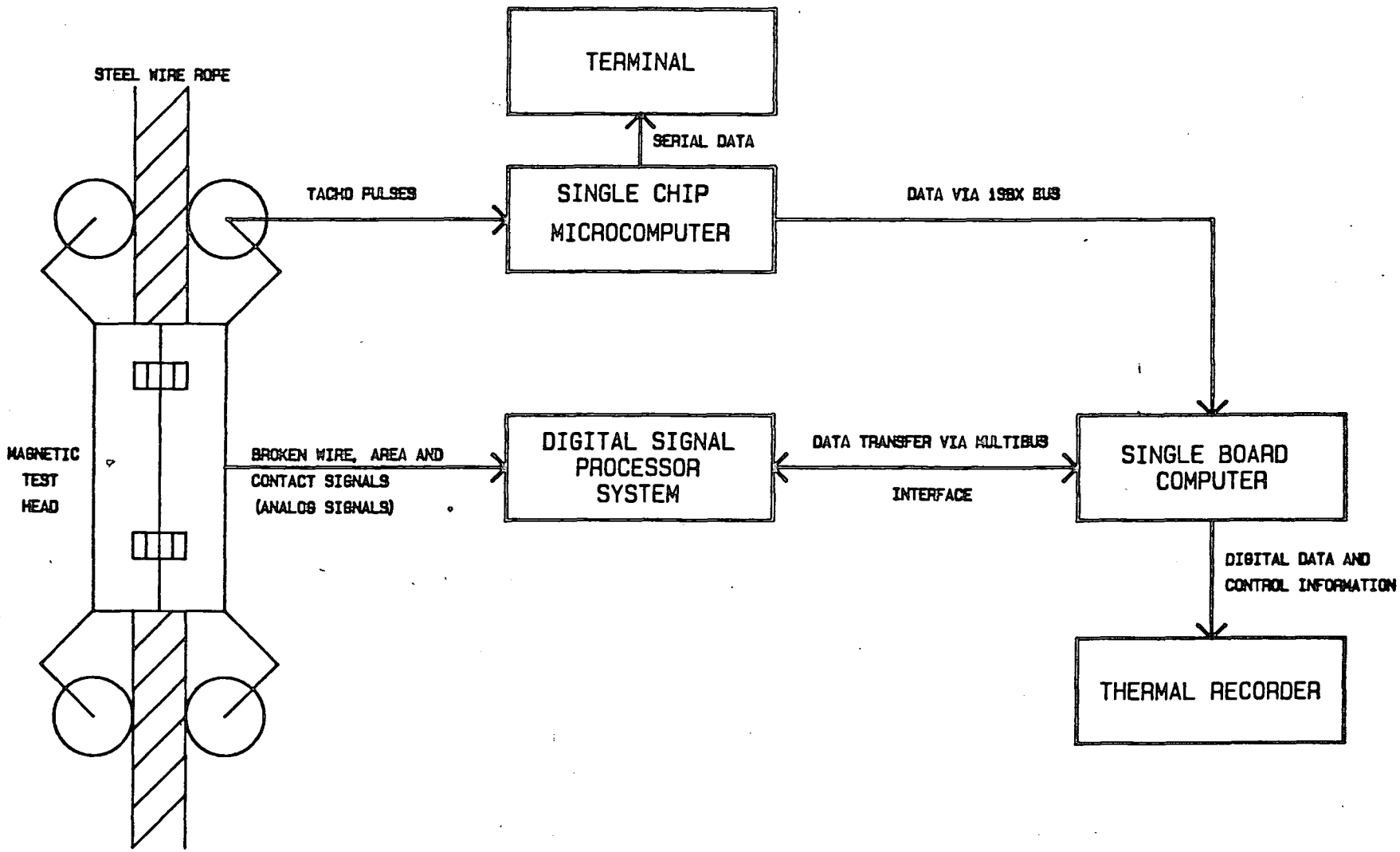


FIGURE 1. SYSTEM CONFIGURATION FOR DIGITAL STEEL WIRE ROPE TESTER

Remove rope noise from the broken wire data.
Signature detection techniques to detect broken wires.
Normalisation of broken wire signal amplitude by correlation of the upper and lower saddle coil voltages.
Integration to determine change in area and change in interwire contact.

Single Board and Single Chip Microcomputer : Calculation of rope speed and distance.
Control of chart recorder.
Printing of data received from the DSP system.
Driving the RS232 terminal.
Perform general "housekeeping" tasks for the system.

Terminal : Display of rope speed, direction of rope travel, rope distance and selection of chart/rope speed conversion ratio.
Serves as operator interface.

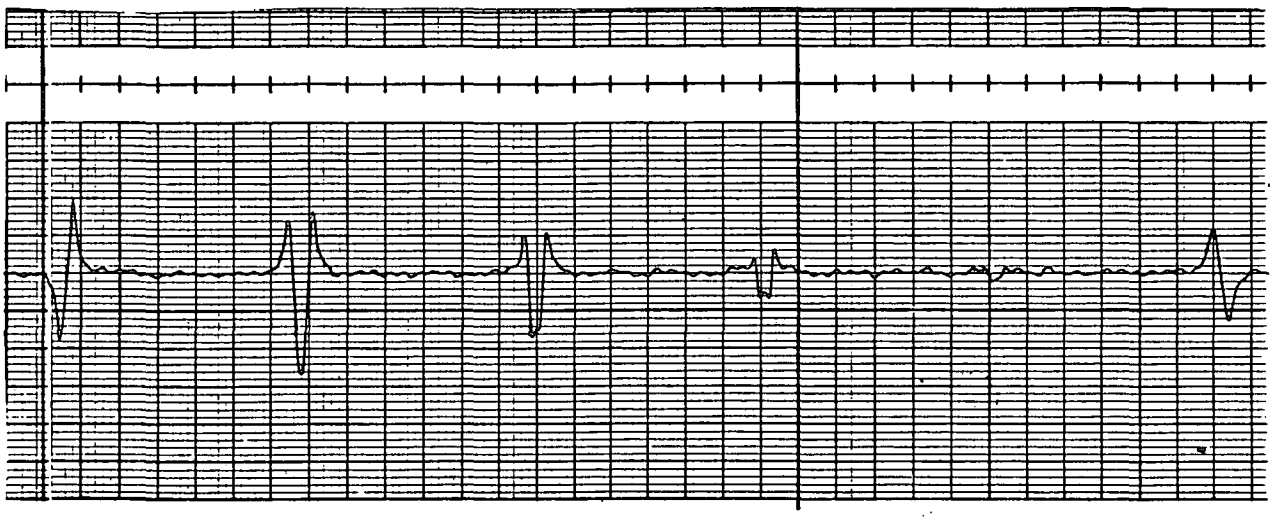
Recorder : Printout of the broken wire, area and contact traces.
Perform certain annotation functions.

1.8 Signal Processing Requirements

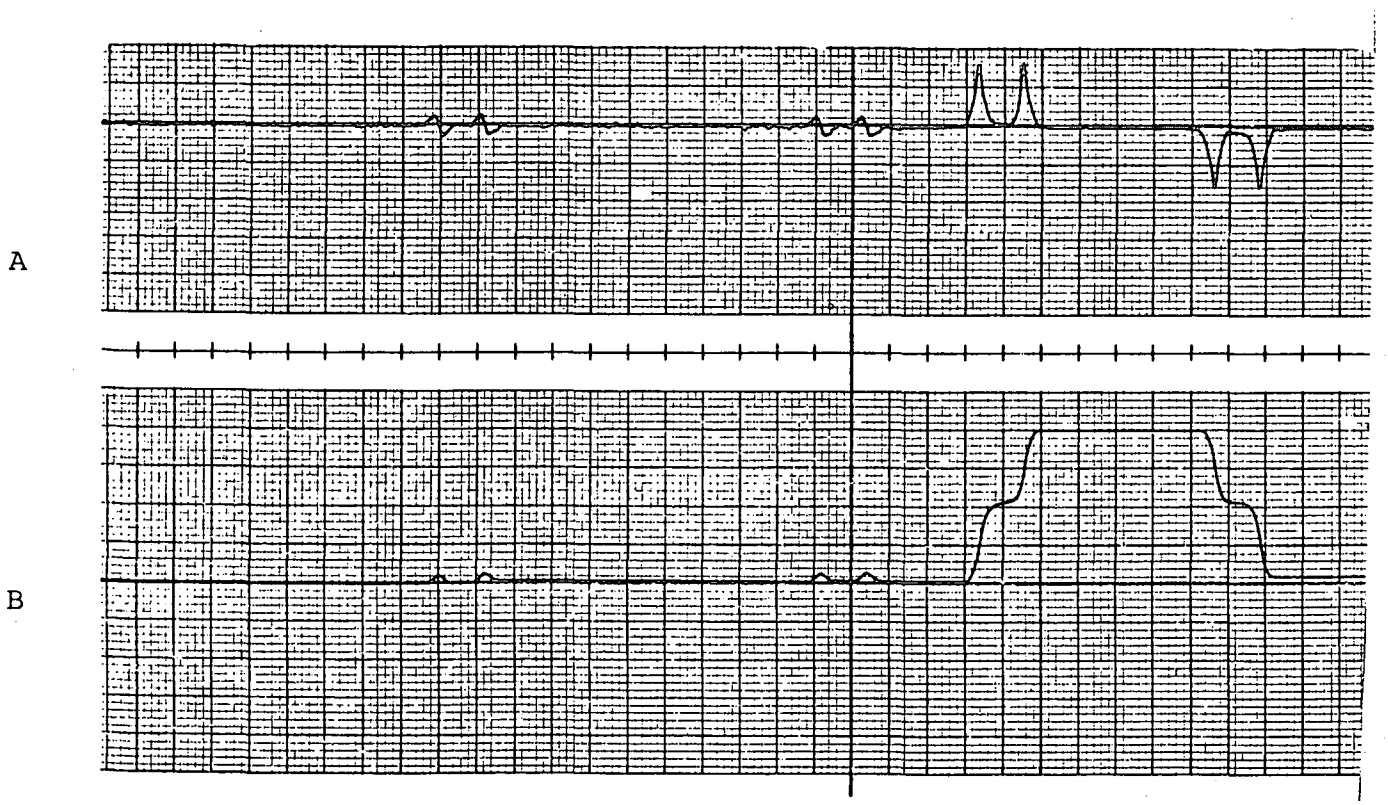
1.8.1 Signal Processing for Broken Wires

The voltage signal induced in the saddle coils of the test head has a characteristic pulse shape. This is shown in Trace 1. The characteristic pulse consists of three peaks with amplitudes which depend on rope speed, break volume and the distance from the sensing coil. Two peaks have approximately equal amplitude with the third peak in the centre of opposite polarity and a larger amplitude. From tests it was determined that a lower limit of 1.3 can be placed on the ratio of the amplitudes. A second criterion must be that the larger peak must exceed the average noise peak amplitude level. Speed corrected signals are then outputted to the single board computer.

The signals from the test head are amplified and then input to the DSP board. The input amplifier must have very low offset voltage otherwise the relationship between the peaks mentioned above will no longer hold true.



TRACE 1



TRACE 2

1.8.2 Signal Proccesing Area and Contact

Both the area and contact saddle coils produce a signal that requires integration. Trace 2(a) shows the area saddle coil output voltage and Trace 2(b) shows the integrated result.
The integrator specifications as determined by Dr N T van der Walt are indicated below.

A. Full scale output for a -12,5 % variation in the nominal cross-sectional area of the rope.

B. Unwanted drift of the output of the integrator over the period of a test must be less than 0.5 % of full scale output.

C. The rope testing instrument must accomodate a range of ropes from 25 mm to 54 mm in diameter.

Requirements A and C are met by choosing the correct gains for the input and output amplifiers. This is dependent on the chart recorder paper size. By choosing amplifiers with very low offsets which after amplification is less than 1 LSB (1.2 mV for a 12 bit A-D converter with a 5V range) drift can be eliminated. Should this be a problem though, techniques have been developed on the TMS32010 evaluation system to compensate for such a problem.

CHAPTER 2

2.0 DESIGN CONSIDERATIONS

Before any real work can commence on the design a number of major decisions have to be made. The major design considerations are summarised below.

1. Which processor to use.
2. Board size.
3. Memory size and types.
4. How much I/O.
5. Expansion facilities.
6. Power requirements.
7. Terminations for I/O.

In addition at each of the above stages is the consideration of cost and availability.

2.1 The Processor

The processor chosen is the TMS320C25. Upward software compatibility was the deciding factor in choosing this processor. The TMS32010 software needs only slight address changes to be able to run on the TMS320C25. This saves on software development and turnaround time in the project. The advanced mathematical capabilities of the TMS320C25 allows easy implementation of complex algorithms. Its 100 ns cycle time enables all three signals to be processed in real time by a single processor. The

Texas Instruments Extended Development Support System was purchased for software and hardware development.

2.2 Board Size

The evaluation system was built around the Multibus standard. In order to maintain hardware and software compatibility it was decided to design the TMS320C25 according to the Multibus standard. The board has to slot in the Multibus rack, so its size and edge connectors have to conform to the mechanical specifications of the Multibus standard.

2.3 Memory

The broken wire signals are to be processed using template comparision techniques. This requires large amounts of memory. There are three signals to be processed and this increases the memory overhead. Therefore 16 kilowords of RAM was chosen. For great flexibility in the software development, 16 kilowords of EPROM was selected.

2.4 Input and Output

There are three signals to be processed from the test head. Therefore an analog multiplexer is used so that all three of these signals can be digitised by a single A-D converter. This arrangement gives lower component count as well as low power

consumption. A 12 bit A-D converter with a 5V range is suitable since it will be able to resolve step changes of at least 1.2 mV.

An eight switch keypad is also required to perform an integrator reset, and operator functions.

The processed data is to be transferred to the single board computer. For the normalisation of the broken wire signal amplitude, the TMS320C25 requires the rope speed. This is achieved by the single board computer conveying this information to the TMS320C25. Bi-directional communication is therefore required. This is implemented via the Multibus bus.

2.5 Expansion Facilities

This is taken care of by the fact that the board is based on the Multibus rack system. Decoding and address mapping is selected via links. This enables up to 8 boards to communicate to the single board computer. Should there be a need for any more processing, it merely involves plugging in the neccessary boards.

2.6 Power Requirements

This is one of the most important considerations since the instrument has to be portable. The evaluation system DSP boards consumed 4,5A each. It is envisaged that with the use of high

speed CMOS this figure can be reduced to 500 mA for the complete DSP board.

2.7 Physical Connections for Input and Output

All I/O enters or leaves the board via finger edge connectors as specified by the Multibus standard.

CHAPTER 3

3.0 INTERFACING MEMORY TO THE TMS320C25

3.1 TMS320C25 Timing and Interface Information

The TMS320C25 implements two seperate and distinct memory spaces:

1) Program space (64 KILOWORDS)
2) Data space (64 KILOWORDS)

Distinction between these two spaces is made through the use of the /PS (program space) and /DS (data space) pins.

A third space, the I/O space is available for interfacing to peripherals. This space is selected by the /IS (I/O space) pin.

3.1.1 Read and Write Cycle Timing (Refer to Figures 2 and 3).

Read cycle:

1. Near the beginning of the machine cycle (CLKOUT1 goes low), the address bus and one of the space signals (/PS,/IS,/DS) becomes valid. R/W goes high to indicate a read cycle.
2. /STRB goes low no less than 13ns after the address bus is valid.
3. Early in the second half of the cycle, the READY input is sampled. READY must be stable no later than 5ns after /STRB goes low.
4. With no wait states (READY is high), data must be available no later than = 27ns after /STRB goes low.

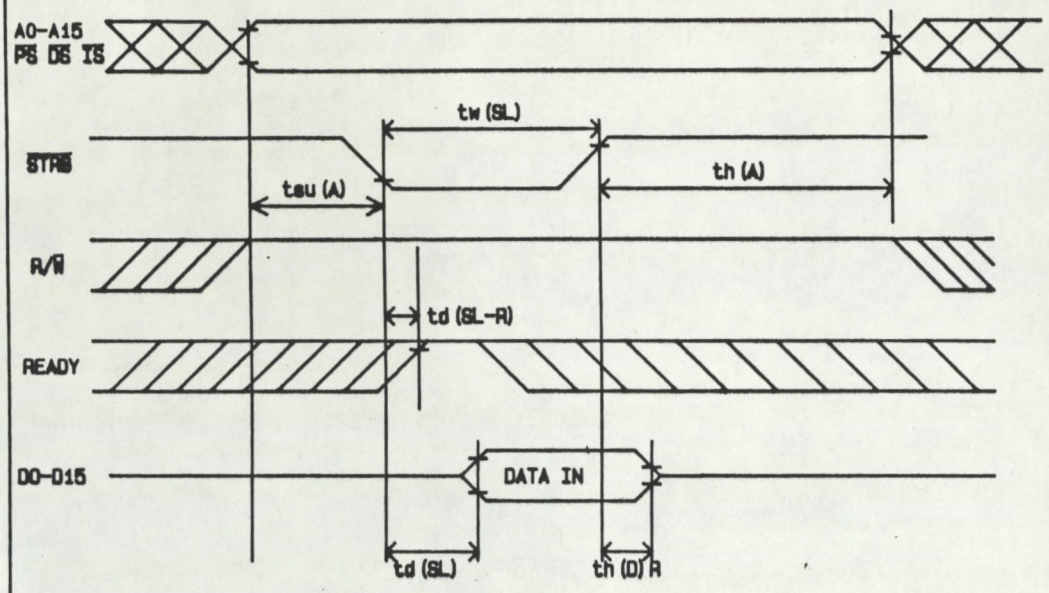
Write cycle:

The sequence of events that occur during the write cycle are the same as the above except for the following differences:

1. R/W goes low to indicate a write cycle.
2. The data bus begins to be driven approximately concurrently with /STRB going low.
3. The data bus enters high impedance state no later than 40ns after /STRB goes high.

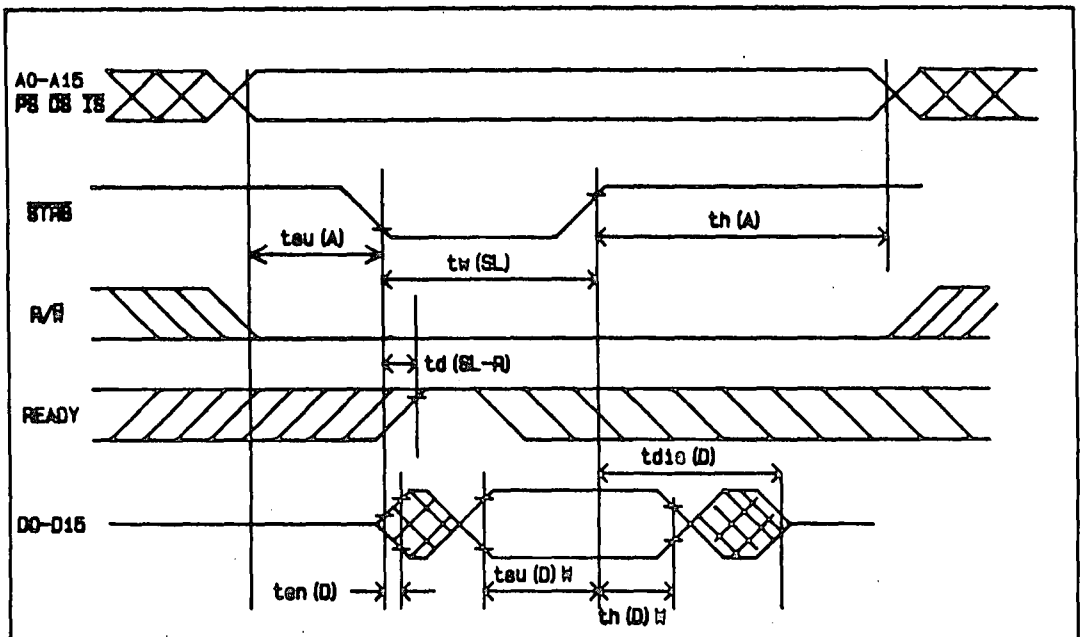
3.2 Wait State Generation

FIGURE 2. TMS320C25 READ CYCLE TIMING DIAGRAM



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	5ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	50ns (typ)
Address Hold Time	th (A)	17ns (min)
Data Setup Time	td (SL)	27ns (max)
Data Hold Time	th (D) R	20ns (max)

FIGURE 3. TMS320C25 WRITE CYCLE TIMING DIAGRAM



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	5ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	50ns (typ)
Address Hold Time	th (A)	17ns (min)
Data Bus Drive Time	ten (D)	15ns (min)
Data Bus Write Setup Time	tsu (D) W	30ns (min)
Data Write Hold Time	th (D) W	15ns (min)
Data Bus Disable Time	tdis (D)	40ns (min)

The READY input allows the capability to interface with memory and peripherals that cannot be accessed in a single cycle. READY must be valid (low or high) no later than 5ns after /STRB goes low. If READY is high then the the memory or peripheral access is completed with the present machine cycle. If READY is low, the access is extended to the next machine cycle, that is a wait state is introduced. The number of wait states required depends on the access time t(a) of that particular memory device or peripheral. If t(a) < 40ns then no wait states are required. If 40ns < t(a) < 140ns one wait state must be inserted. In general, N wait states are required for a particular access if [100(N-1) +40]ns < t(a) < [100N + 40]ns.

The number of wait states required for a memory or peripheral access is summarised below.

Access Time	Number of Wait States Required
t(a) < 40ns	0
40ns < t(a) < 140ns	1
140ns < t(a) < 240ns	2
240ns < t(a) < 340ns	3
340ns < t(a) < 440ns	4

3.3 Data Memory Space Interface

Memory requiring 0 wait states for interfacing was chosen for maximum throughput. The device chosen was the Saratoga Semiconductor SSM7164-35 static RAM integrated circuit. This device has an address access time of 35ns maximum.
Figures 4 and 7 show the hardware associated with data space memory.

3.3.1 Processor and Decoding Circuits

The processor and decoding circuits are shown in Figure 4.
The processor has three address strobe signals.
These signals are used to enable to the decoders in the program space, data space and input/output space. 74AS138 decoders are used throughout the decoder design. In order to generate the /OE signal and /WE signal an inverter and OR gates are used. Note that Advanced Schottky devices are used because they have very low propogation delay times. For zero wait state operation at 40MHz operation, even adding a single logic gate in the signal path can render a design unworkable.

3.3.2 Data Memory Circuit

The circuit is shown in Fiqure 7. The memory devices used here are the SSM7164-35. They are U22, U23, U26 and U27. These devices have data output enable times of 15 ns and address access times of 35 ns. Together with the processor and decoding section no other devices are used for this interface.

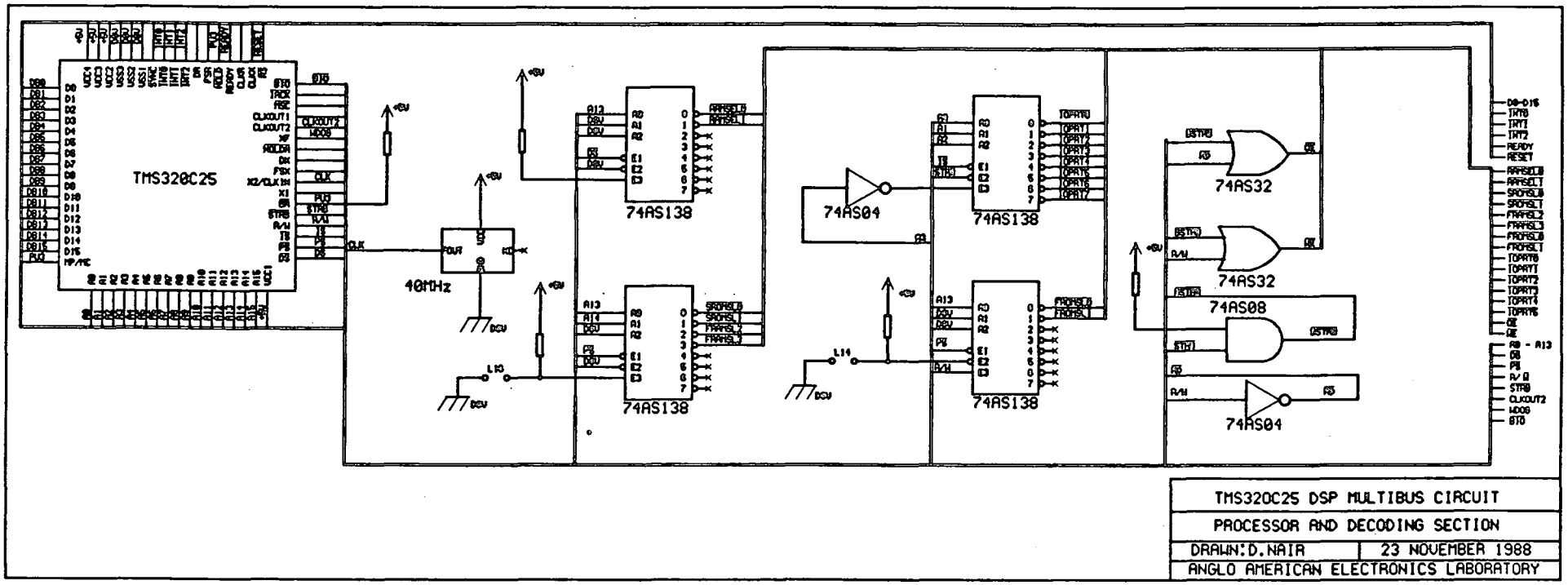

TMS320C25
40MHz
74AS138
74AS138
74AS04
74AS138
74AS138
74AS32
74AS32
74AS08
74AS04
TMS320C25 DSP MULTIBUS CIRCUIT
PROCESSOR AND DECODING SECTION
DRAWN:D.NAIR
23 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 4

3.3.3 Read Cycle Timing of the SSM7164-35 (Refer to Fiqure 5).

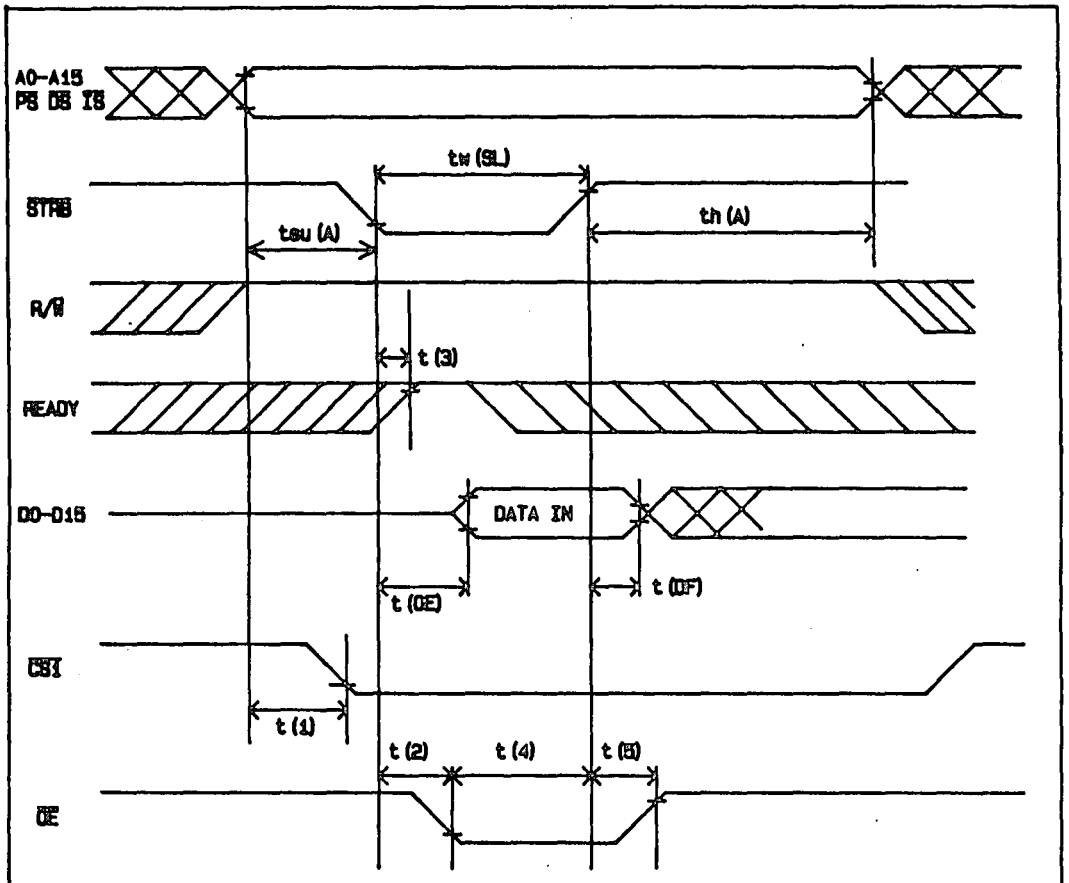
In a read cycle, read/write (R/W) goes high concurrently with a valid address, indicating a read rather than a write cycle has been initiated. With data strobe (/DS) used to enable the 74AS138 /RAMSEL0 or /RAMSEL1 goes low no later than t(1) = 10ns after address is valid. This is the maximum propogation delay through the 74AS138. Output enable (/OE) goes low after a maximum time of t(2) = 11,6ns after /STRB goes low.

The SSM7164-35 begins driving the bus no later than 15ns after /OE goes low, [t(oe)=15ns]. Therefore the worst case access time is t(2) + t(oe) = 11,6ns + 15ns = 26,6ns. This meets the 27ns access time required by the TMS320C25 operating at 40MHz.

The READY input is driven by a 74AS10, 3 input NAND gate by the /DS signal. READY is high 5ns [t(3)] after /DS goes low or after the address is valid. This meets the 18ns requirement for READY to be valid after address valid for the TMS320C25 operating at 40MHz.

After /STRB goes high the SSM7164-35 enters high impedance state within 26,6ns maximum, thus avoiding bus conflict if a read cycle is followed by a write cycle.

FIGURE 5. READ CYCLE OF SSM7164-35



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after Address	t (3)	5ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	50ns (typ)
Address Hold Time	th (A)	17ns (min)
Propogation Delay -74AS138	t (1)	10ns (max)
Progation Delay -74AS08 and		
74AS32	t (2)	11, 6ns (max)
$\overline{\text{STRB}}$ Low to Data Valid	t (OE) +t (2)	26, 6ns (max)
$\overline{\text{STRB}}$ High to Data Float	t (DF) +t (5)	26, 6ns (max)

3.3.4 Write Cycle Timing of SSM7164-35 (Refer to Fiqure 6).

As shown in the timing diagram, the memory write cycle is similar to read cycle with the exception that R/W is low.
The TMS320C25 begins driving the bus as soon as /STRB goes low while /WE follows within 10ns.

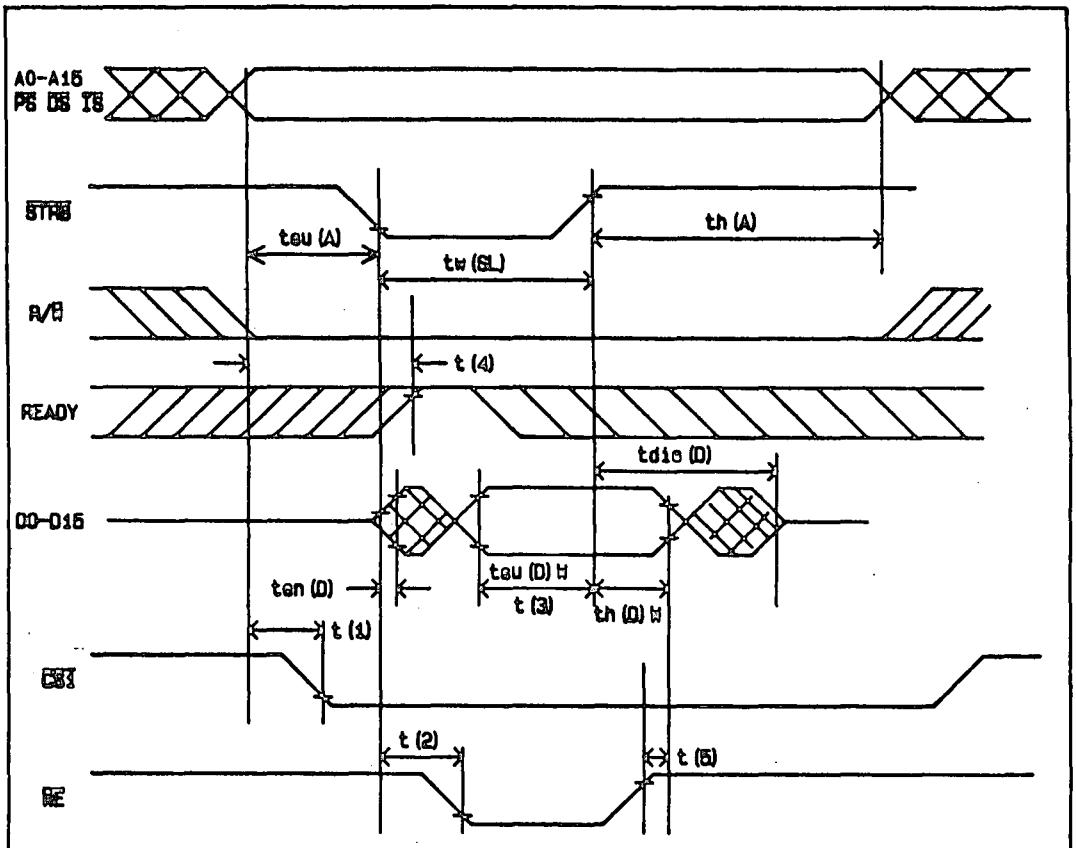
Data is clocked into the SSM7164-35 by the rising edge of /WE. This time is no less than the TMS320C25 minimum data setup time before /STRB goes high which is 30ns plus the maximum propogation delay = t(2) = 11,6ns. Therefore the actual setup time is 41,6ns. Note that this time meets the minimum data setup time required by the SSM7164-35.

3.4 Program Memory Space Interface

The circuit diagram is shown in Figures 4 and 7.
Because it may be difficult to obtain reprogrammable memory devices that are capable of being operated at zero wait state with the TMS320C25 running at a clock speed of 40MHz it was decided to design in the following two options:

1. 16 kilowords of high speed RPROM (0 wait state operation) mapped in lower 16K (0 - 3FFF).
2. 16 kilowords of standard 27C128 EPROM (1 or 2 wait state operation) mapped in the same lower 16K (0 - 3FFF) as the high speed RPROM. 16K of high speed

FIGURE 6. WRITE CYCLE TIMING OF SSM7164-35



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after Address	t (4)	5ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	50ns (typ)
Address Hold Time	th (A)	17ns (min)
Data Bus Drive Time	ten (D)	15ns (min)
Data Bus Write Setup Time	tsu (D) W	30ns (min)
Data Write Hold Time	th (D) W	15ns (min)
Data Bus Disable Time	tdis (D)	40ns (min)
Propogation Delay -74AS138	t (1)	10ns (max)
Propogation Delay -74AS138		
and 74AS32	t (2)	11.6ns (max)
Data Hold Time after $\overline{\text{WE}}$ High	t (5)	5.4ns (min)

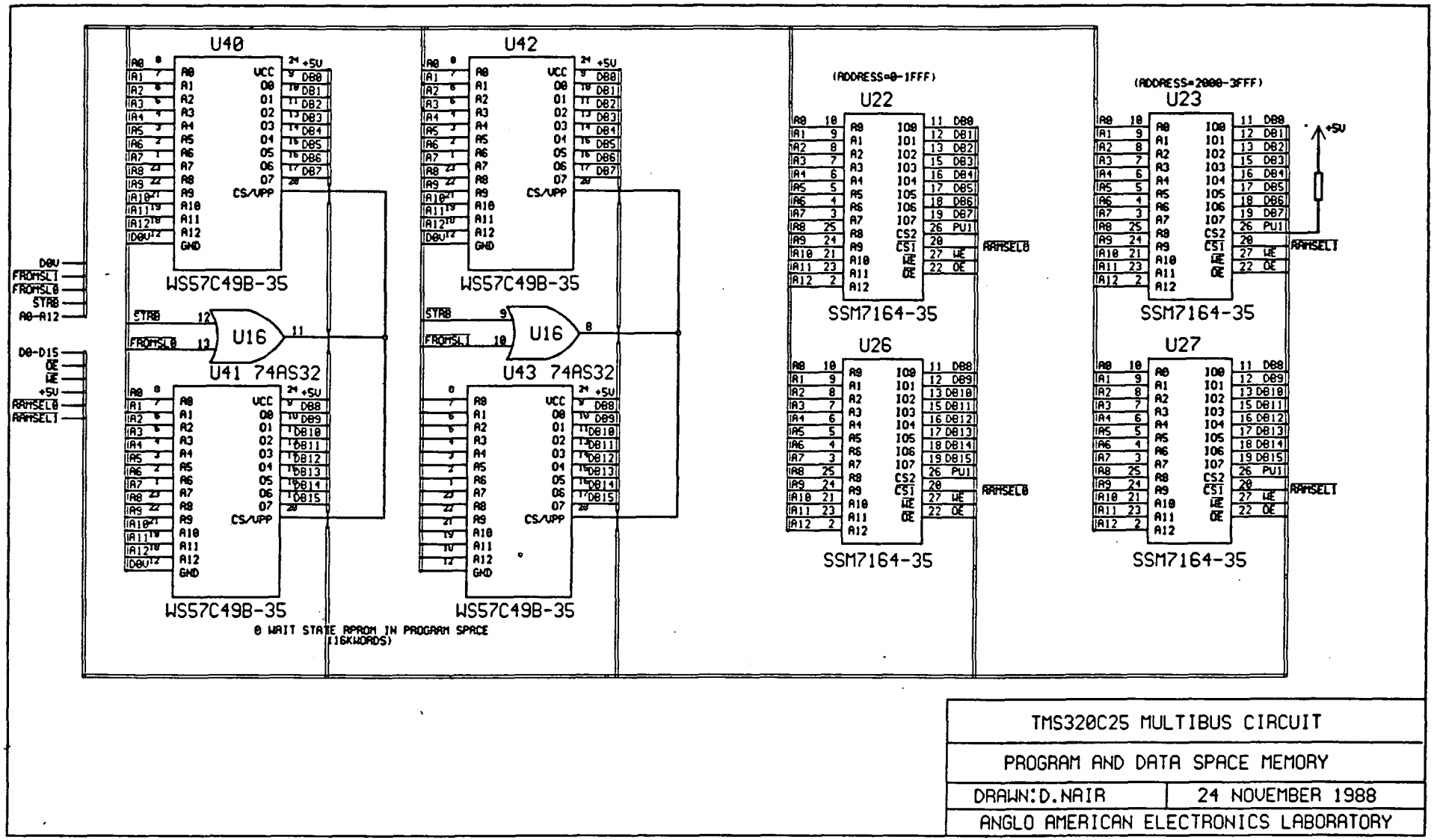

U40
U42
U22
U23
U26
U27
U16
U41 74AS32
U43 74AS32
WS57C49B-35
SSM7164-35
(ADDRESS=0-1FFF)
(ADDRESS=2000-3FFF)
+5V
D0V
FROMSLT
FROMSLO
STRB
A0-A12
D0-D15
OE
WE
RAMSELO
RAMSELT
0 WAIT STATE RPROM IN PROGRAM SPACE
(16KWORDS)
TMS320C25 MULTIBUS CIRCUIT
PROGRAM AND DATA SPACE MEMORY
DRAWN: D.NAIR
24 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 7

static RAM (0 wait state) mapped from 4000 to 3FFF.

Should the high speed RPROM be available, then the memory devices in the second option should be removed from the printed circuit board or disabled by the appropriate links. Otherwise the two 27C128's can be utilised by making use of the TBLR and TBLW commands of the TMS320C25. These commands make it possible to copy a block of object code from the slow EPROM to the high speed RAM mapped in the program space. Therefore maximum throughput would still be maintained, although the power up initialisation will be slower. This method has definite economic advantages considering that the high speed RPROM costs about R130 each.

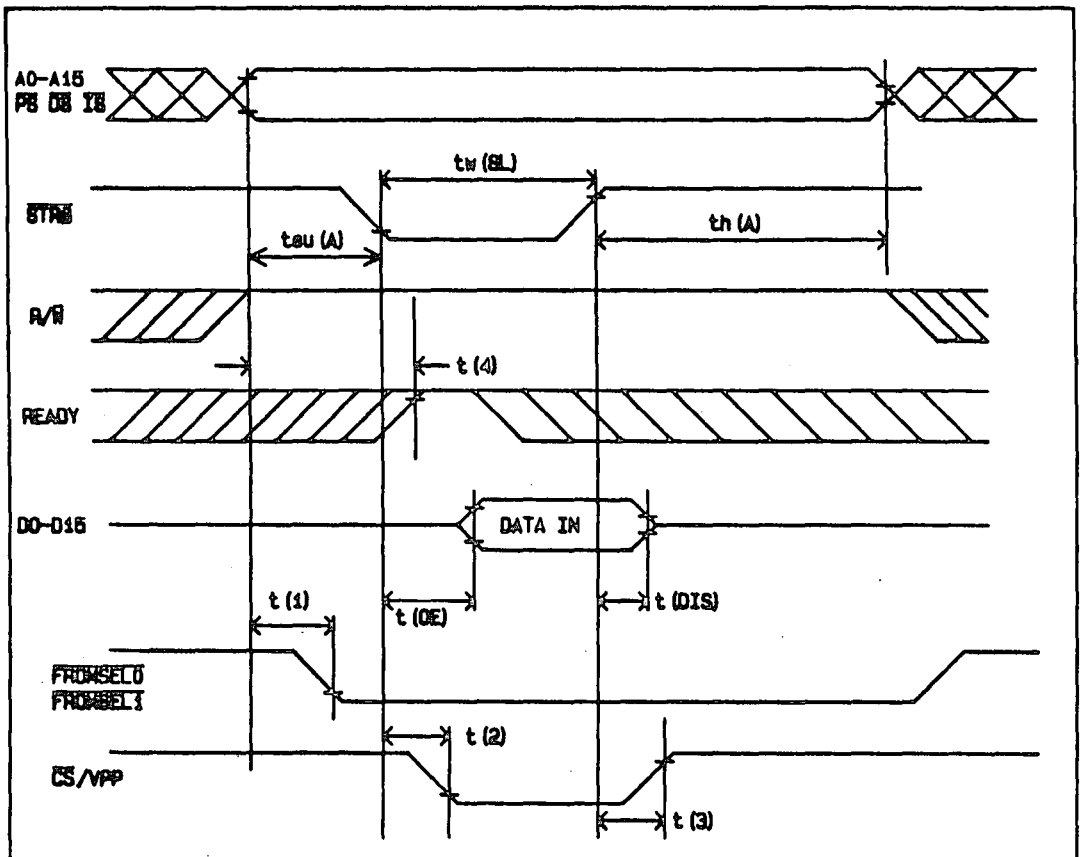
The devices chosen for this section are listed below:

Device		Address Access Time
EPROM 27C128	(1 wait state)	40ns < t(a) < 140ns
EPROM 27C128	(2 wait state)	140ns < t(a) < 240ns
RAM SSM7164-35	(0 wait state)	t(a) = 35ns
RPROM WS57C49B-35	(0 wait state)	t(a) = 35ns

3.4.1 Read Cycle Timing of WS57C49B-35 (Refer to Fiqure 8).

In a read cycle, R/W goes high concurrently with a valid address, indicating a read rather than a write cycle has been initiated. With /PS used to enable the 74AS138 /FROMSEL0 or /FROMSEL1 goes low no later than t(1) = 10ns

FIGURE 8. READ CYCLE TIMING OF WS57C49B



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after Address	t (4)	17, 4ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	50ns (typ)
Address Hold Time	th (A)	17ns (min)
Data Setup Time	t (OE)	25, 8ns (max)
$\overline{\text{STRB}}$ High to Data Float	t (DIS)	25, 8ns (max)
Propogation Delay -74AS138	t (1)	10ns (max)
Propogation Delay -74AS32	t (2)	5, 8ns (max)
Propogation Delay -74AS138	t (3)	10ns (max)

after address is valid. This is the maximum propogation delay through the 74AS138. The memory select signals are gated with the /STRB signal. 5.8ns after /STRB goes low one of the /CS,VPP signals goes low, selecting a particular pair of RPROMS.

The WS57C49-35 drives the bus with valid data no later than 20ns after /CS,VPP goes low, [t(oe)=20ns]. Therefore the worst case access time is t(2) + t(oe) = 5,8ns + 20ns = 25,8ns after /STRB goes low. This meets the 27ns access time required by the TMS320C25 operating at 40MHz. The address access time is t(acc) = t(/STRB) + t(PLH)74AS32 = 13ns + 5,8ns = 18,8ns which meets the address setup time 15ns mimimum before /CS goes low.

Note the R/W signal is also used to enable the 74AS138 in the program space. This is done to prevent selecting the RPROM during a write cycle. Should this occur it is possible that the memory device and the processor could be damaged.

The READY input is driven by a 74AS10, 3 input NAND gate by the /PS signal via a 74AS04 and a 74AS00 gate. Link L18 is removed and L13 is inserted for this option. Ready is high 14 ns after address is valid [t(PLH)74AS04 + t(PLH)74AS00 + t(PLH)74AS10 = 5ns + 4,5ns + 4,5ns = 14ns]. This meets the 18ns requirement for READY to be valid after address valid for the TMS320C25 operating at 40MHz. This arrangement for generating the READY signal was neccessary because of the various memory options designed in and the need for such a scheme will become clearer once the wait state generator and the slower memory section is described.

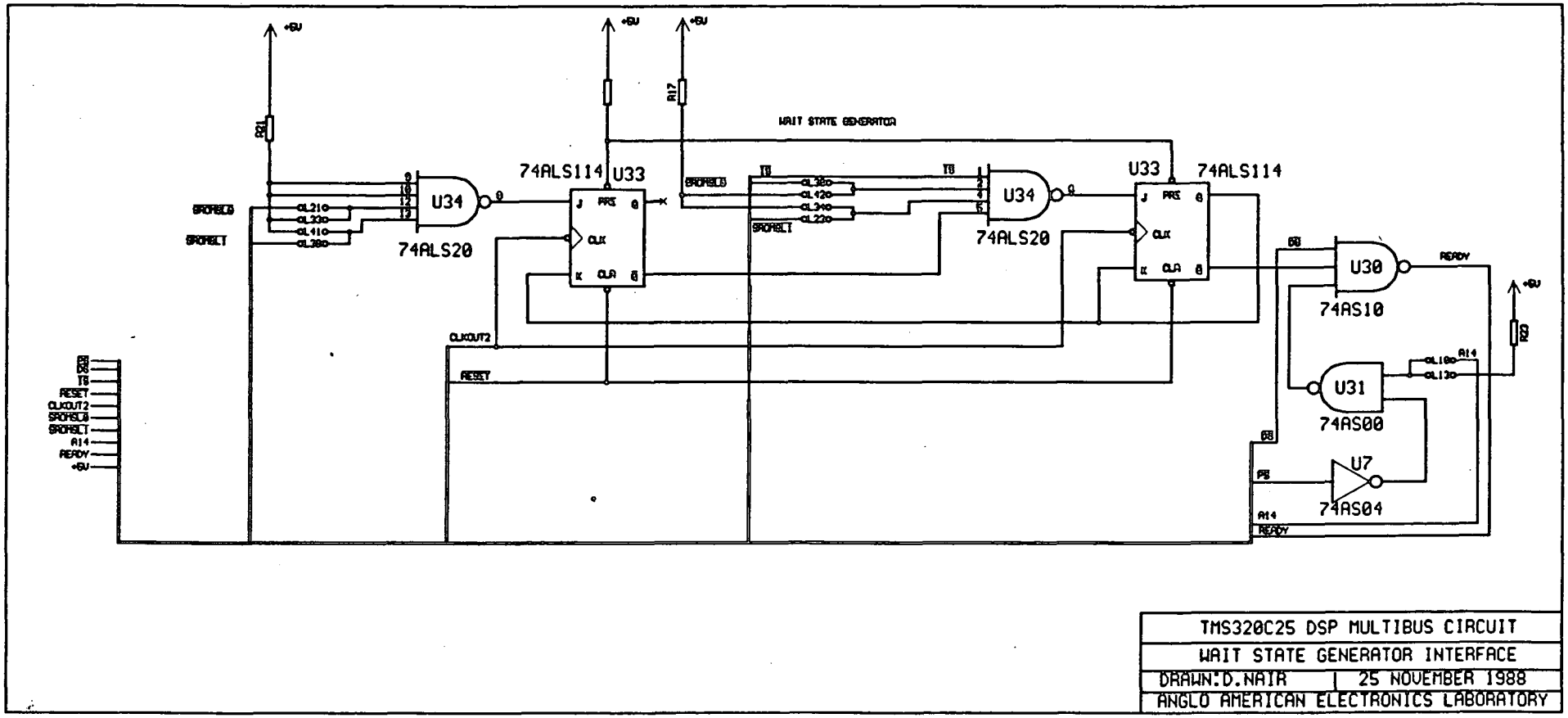

WAIT STATE GENERATOR
74ALS114
U33
74ALS20
U34
74AS10
U30
74AS00
U31
74AS04
U7
TMS320C25 DSP MULTIBUS CIRCUIT
WAIT STATE GENERATOR INTERFACE
DRAWN: D.NAIR
25 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 9

After /STRB goes high the WS57C49B-35 enters high impedance state within a maximum time of t(3) + t(DIS) = 5,8ns + 20ns = 25,8ns. Therefore, no bus conflict occurs if the present read cycle is followed by a write cycle.

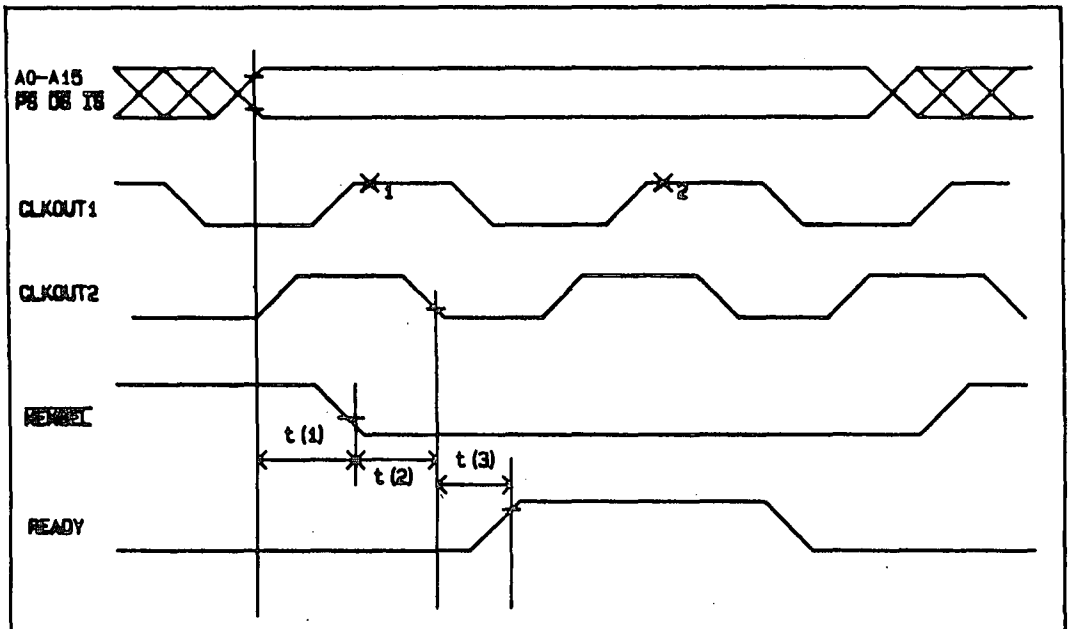
3.4.2 The Wait State Generator

The wait state generator design is shown in Fiqure 9 and timing in Figures 10 and 11.

The design utilizes a 74ALS114A dual J-K flip-flop. Both these flip-flops are clocked by the CLKOUT2 signal of the TMS320C25. First consider the case of one wait state. Time t(1) in Figure 10 is the time from address valid to memory select of the particular device that requires the wait state. This corresponds to the propogation delay through the address decode logic. For a 74AS138 decoder, t(1) = 10ns maximum. The memory select of the device is connected to one of the inputs of the second NAND gate as shown in Figure 9. When memory select goes low, the output of the second NAND gate goes high. At the second flip-flop, J=1 and K=0; that is the flip-flop will be set when CLKOUT2 goes low, and the TMS320C25 enters a wait state.

Consider time t(2) in Figure 10. This is the time from memory select going low to CLKOUT2 going low. Time t(2) must be greater than the maximum propogation delay t(PLH) of the 74ALS20 and the setup time of the J-K flip-flop, i.e., t(PLH)74ALS20 + t(su)74ALS114 = 11ns +20ns = 31ns. The time for a valid address to CLKOUT2 going low is 63ns mimimum (13ns minimum setup time for

FIGURE 10. TIMING OF WAIT STATE GENERATOR
ONE WAIT STATE



X1 = Point at which Ready is sampled for first time.
X2 = Point at which Ready is sampled for second time.

SIGNAL DESCRIPTION	SYMBOL USED	VALUE
MEMSEL Low to Ready High	t (2)	53ns
Propogation Delay -74AS138	t (1)	10ns (max)
Propogation Delay -74ALS114		
and 74AS10	t (3)	24ns (max)

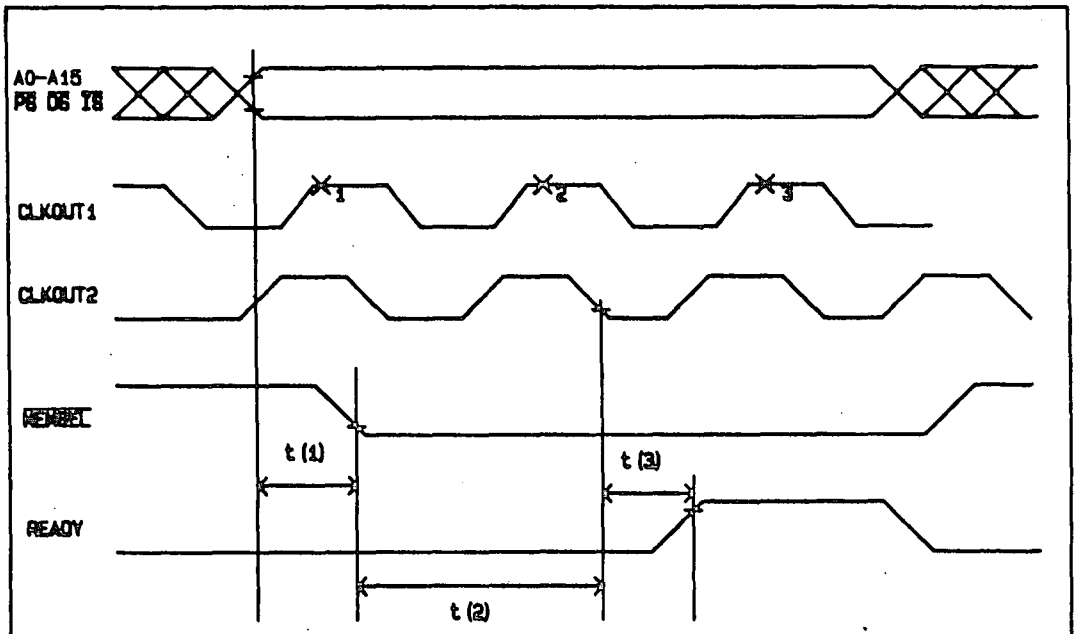
the address plus 50ns for CLKOUT2 high. If a 74AS138 (10ns maximum propogation delay) is used for address decoding, t(2) = 63ns -10ns = 53ns; therefore, t(2) > 31ns. This implies that the maximum progation delay of the address decoding logic is limited to 63ns -31ns = 32ns.

When CLKOUT2 goes low, the second flip-flop is set, i.e., Q=1 and /Q=0. Since /Q drives one of the inputs of the 74AS10, READY (output of 74AS10) goes high. Time t(3) in Figure 11 is the time from CLKOUT2 going low to READY going high. The READY input to the TMS320C25 must be valid 55ns after CLKOUT2 goes low (50ns for CLKOUT2 low plus 5ns for CLKOUT2 going high and READY valid). Therefore t(3) must satisfy the requirement: t(3) < 55ns. The maximum propogation delays through the 74ALS114 and the 74AS10 are 19ns and 5ns respectively. Therefore, t(3) = 24ns (max), satisfying the 55ns requirement.

READY must be high until it is sampled again, shortly after CLKOUT1 goes high. In the design of Figure 9, READY remains high well after CLKOUT1 goes high. At the falling edge of CLKOUT2, the inputs of the J-K flip-flop are J=1 K=Q=1, and the flip-flop is in the toggle mode. When CLKOUT2 goes low, /Q goes back to logic 1. READY goes low and stays low until one of the inputs of the 74AS10 is pulled low.

To implement two wait states, a second J-K flip-flop is utilized as shown in Fiqure 9. This delays READY going high by an additional machine cycle. The timing diagram of the two wait state generator is shown in Fiqure 11.

FIGURE 11. TIMING OF WAIT STATE GENERATOR
TWO WAIT STATES



X1 = Point at which Ready is sampled for first time.
X2 = Point at which Ready is sampled for second time.
X3 = Point at which Ready is sampled for third time.

SIGNAL DESCRIPTION	SYMBOL USED	VALUE
$\overline{\text{MEMSEL}}$ to Ready High	t (2)	103ns
Propogation Delay -74AS138	t (1)	10ns (max)
Propogation Delay -74ALS114		
and 74AS10	t (3)	24ns (max)

3.4.3 27128s EPROM Interface in Program Space

The circuit diagram is shown in Fiqure 12.
The 27C128s can be operated with either 1 or 2 wait states. Depending on the access time of the device chosen, the appropriate links are either inserted or removed according to Table 1.

The 27C128s are mapped from 0 to 3FFF because the reset vector points to location 0000 on /RESET. A seperate decoder is used in this section so that the decoder ICs do not haved to be removed from the board but can be simply selected or deselected by the insertion or removal of links.

The /CE signal of the 27C128s is obtained by ANDing the two memory select signals /SROMSL0 and /SROMSL1. This is because the 74AS138 decoder is used to decode blocks of eight kilowords whereas the 27C128 contains a 16 kilobyte of memory each. This decoding scheme is used because the high speed RAM used mapped into the program space is only available in blocks of eight kilobytes wide.

3.4.3 Read Cycle Timing of 27128s with Wait States

The option of using 1 or 2 wait state EPROM was chosen because devices are available which can be run at either 1 or 2 wait states. For some applications where maximum throughput is of little consequence the entire object code can be run from the 2

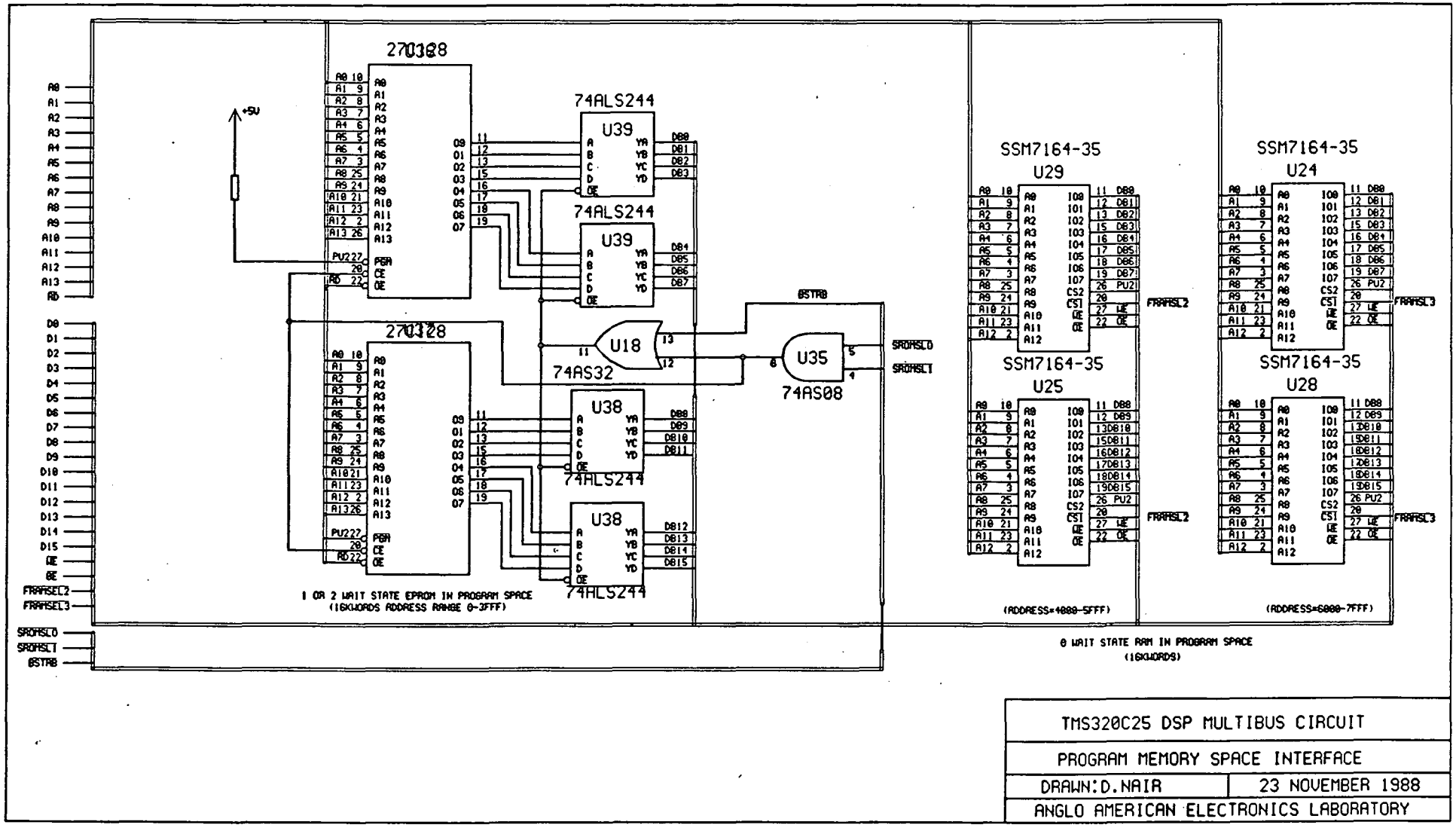

27C128
74ALS244
U39
74ALS244
U39
27C128
U18
74AS32
U35
74AS08
74ALS244
U38
74ALS244
U38
SSM7164-35
U29
SSM7164-35
U24
SSM7164-35
U25
SSM7164-35
U28
BSTRB
SROMSL0
SROMSL1
FRAMSEL2
FRAMSEL3
1 OR 2 WAIT STATE EPROM IN PROGRAM SPACE
(16KWORDS ADDRESS RANGE 0-3FFF)
(ADDRESS=4000-5FFF)
(ADDRESS=6000-7FFF)
0 WAIT STATE RAM IN PROGRAM SPACE
(16KWORDS)
TMS320C25 DSP MULTIBUS CIRCUIT
PROGRAM MEMORY SPACE INTERFACE
DRAWN:D.NAIR
23 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 12

wait state EPROM; this may be a more cost effective solution depending on the application.

In the description of this section of the program space; 27C128s with an access time of 200 ns would be handled; this being the more commonly used device and also requiring a description of the timing associated with the TMS320C25 running at its slowest speed of two wait states.

With an access time of 200 ns two wait states are needed. These are implemented using the wait state generator described previously. The memory cycle starts with address valid. /SROMSL0 or /SROMSL1 becomes low 10 ns maximum later (this is the propogation delay through the 74AS138).
/CE of 27C128 goes low after a maximum time of 15,5 ns after valid address [t(PHL)74AS138 + t(PHL)74AS08 = 10 ns + 5,5 ns = 15,5 ns]. The 74ALS244 octal buffers are used to buffer the memories from the TMS320C25. These buffers are enabled by the logical-OR of memory select and /BSTRB (buffered /STRB signal since the /STRB signal can only sink sufficient current for only 4 AS logic type gates). The maximum propogation delay through the buffers is t(p) = 10 ns. Therefore valid data appears on the bus no later than
t(3) = t(1) + t(a) + t(p) + t(74AS08) +t(74AS32) = 10 ns +
200 ns + 10 ns + 5,5 ns + 5,8 ns = 231,3 ns from valid address. This is the overall access time, and
140 ns < t(3) < 240 ns; i.e., two wait states are sufficient. The generation of the READY signal would follow the operation of the wait state generator and would therefore not be repeated.

With /STRB going high, the TMS320C25 has completed the memory read. The output enable of the 74ALS244 would follow /STRB after a maximum time of 11,3 ns [t(PLH)74AS08 + t(PLH)74AS32 = 5,5 ns + 5,8 ns = 11,3 ns]. This forces the 74ALS244s to enter high impedance state 13 ns maximum later. Therefore, no later than 11,3 ns + 13 ns = 24,3 ns after /STRB goes high, the outputs of the 74ALS244s are in a high impedance state. Buffers were used because the disable time of the memory is 55ns which would generate a conflict on the data bus. Data output turnoff is an important parameter and must be taken into consideration when designing with high speed microprocessors.

3.4.4 Static RAM in Program Space

The static RAM device used is the same as the device used in the data memory space, the SSM7164-35 requiring zero wait states. The only difference in the interfacing of this device is the memory select signals and the READY signal generation. The timing diagram is the same as the data memory interface and will not be described again.

For this option consult the link selection table for the memory devices used and set accordingly. The memory select signals /FRAMSL2 and /FRAMSL3 are taken from the program space decoder.

Once RAM in the address space 4000 to 7FFF is selected address line A14 would be high. A14 together with the /PS signal is used to generate the READY signal. With the gating arrangement shown in the wait state generator circuit diagram, READY is high no later than t(PHL)74AS04 + t(PHL)74AS00 + t(PLH)74AS10 = 5 ns + 4,5 ns + 4,5 ns = 14 ns which meets the requirement for the 0 wait state operation of the TMS320C25 operating at 40MHz. (14 ns < 18 ns).

MEMORY SELECTION AND WAIT STATE GENERATION

	t(a)<40ns	t(a)<140ns	t(a)<240ns
LINK NAME	0 WS RPROM	1 WS EPROM	2 WS EPROM
L13	IN	OUT	OUT
L18	OUT	IN	IN
L42	IN	OUT	IN
L30	OUT	IN	OUT
L23	OUT	IN	OUT
L34	IN	OUT	IN
L38	OUT	OUT	IN
L41	IN	IN	OUT
L33	IN	IN	OUT
L21	OUT	OUT	IN
L16	OUT	IN	IN
L14	IN	OUT	OUT

t(a) = access time
WS = wait state
EPROM = 27C128 EPROM
RPROM = WS57C49B-35

TABLE 1

CHAPTER 4

4.0 DATA ACQUISITION SECTION

On the evaluation system the integrators ran on a sample frequency of 32KHz. The DSP board needs to integrate two signals. For only these two channels to be processed we need a maximum sample rate of 64KHz. The broken wire signals need a sample rate of at least 2KHz. For all three channels to be processed we require at least 66KHz. It was decided that for greater flexibilty of the system, a sample rate of at least 125KHz is required. This means that the other five channels on the board can be used for other applications without any problems with sample rates. The maximum sampling rate is determined by the following equation:

$$F(max) = 1/[T(acq) + T(aper) + T(conv)]$$

where T(acq) = acquisition time of sample and hold
T(aper) = aperture time of sample and hold
T(conv) = conversion time of analog-to-digital converter
F(max) = maximum sampling frequency

For a 125KHz maximum sampling rate, and selecting the MAX162 3us A/D converter, the maximum allowable sum of the aperture and acquisition time = 5us. The sample and hold selected was the AD585 which has an acquisition time of 3us and a aperture time of 35ns.

The Nyquist theorem states that a bandwidth-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information.

Thus the maximum input signal frequency is given by the following equation:

$$Finput(max) = \frac{1}{2}/[T(acq) + T(conv) + T(aper)]$$

where Finput(max) = maximum input signal frequency and the other symbols are as defined above.

Using the MAX162 and the AD585, F(max) = 125KHz. This is adequate because the A-D has convert up to 8 analog channels. The high sampling rate is required to reduce errors in the integral computations. The algorithm used for integration is based on the trapezoidal rule. Therefore a higher sampling rate would give a smaller error in the result of the integration.

Another factor affecting the accuracy of the conversion is the droop rate of the sample and hold. Droop is the change in output voltage from the "held" value as a result of device leakage. The voltage at the output of the sample and hold should ideally be held constant for the entire duration of the conversion. However, this voltage does change in accordance with the droop rate of the sample and hold. For minimum error the total droop in the output voltage has to be less than 1/2 LSB during the period of a conversion. The maximum allowable signal change on the input of the A/D converter is:

Change in V = FSR/[2 to the power (N + 1)]

where FSR = full scale range

N = number of bits

Change in V = change in voltage at the input of the A/D

The maximum allowable change at the input of the A/D for a 5V full scale range is therefore 610uV. The AD585 has a maximum droop rate of 1mV/ms. The conversion time of the MAX162 is 3us. Therefore the voltage at the input of the A/D would have changed by 3uV at the end of a conversion. This is much less than 610uV.

4.1 Analog Multiplexer and Channel Selection (Refer to Figure 13).

There are three signals to be processed by the digital signal processor. These are the broken wire, area and contact signals. To enable a single processor to process all these signals an analog multiplexer was implemented in the front end. This multiplexer is a high accuracy instrumentation amplifier capable of switching speeds up to 200KHz. It is specified to settle to within 0,01% of its final value in a maximum time of 3us with a full scale voltage applied at the input. The analog multiplexer is an eight channel device.

Channel selection is performed by a register mapped in the I/O space. The address inputs of the multiplexer is driven by open collecter AND gates to perform level shifting neccessary because

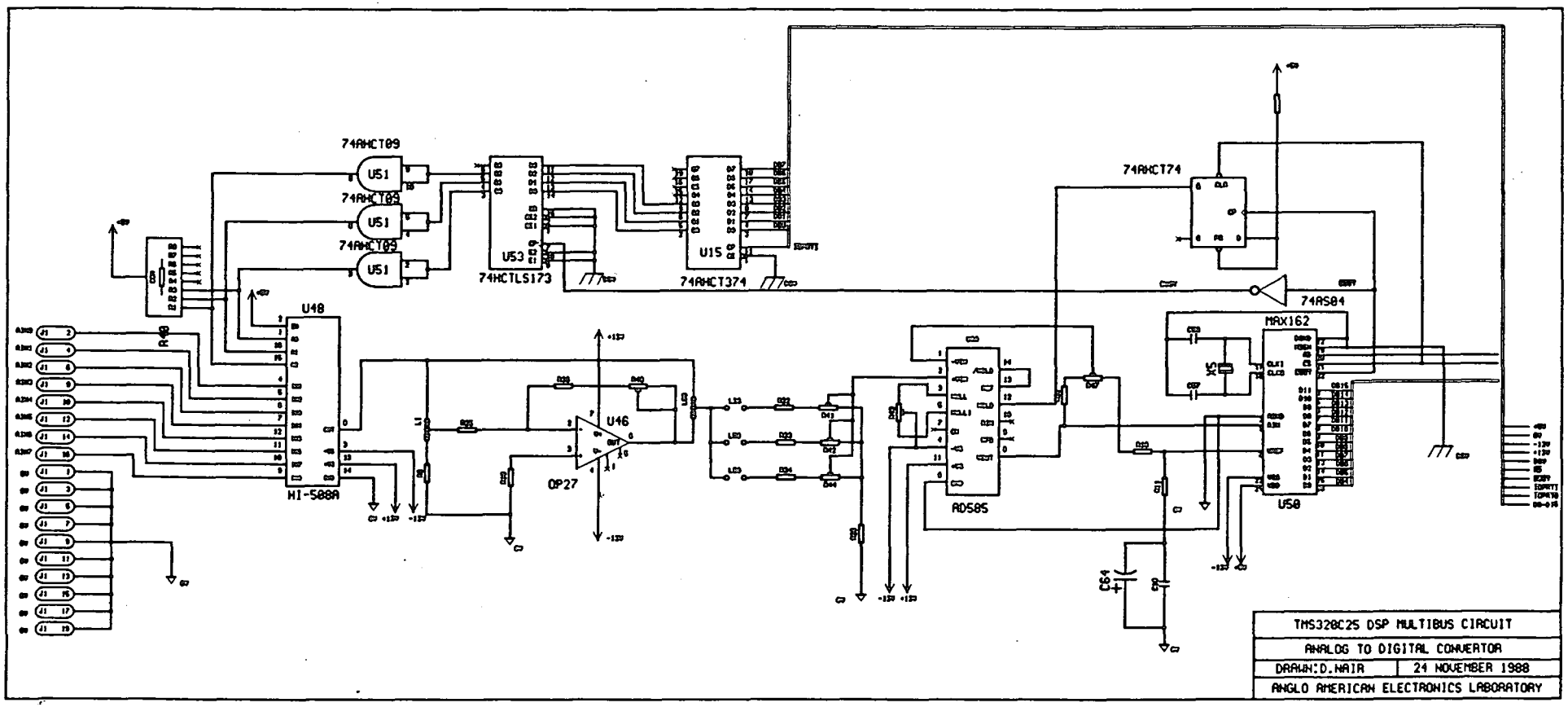

74AHCT09
U51
74AHCT09
U51
74AHCT09
U51
U53
74HCTLS173
U15
74AHCT374
74AHCT74
74AS04
MAX162
U48
HI-508A
U46
OP27
AD585
U50
C64
TMS320C25 DSP MULTIBUS CIRCUIT
ANALOG TO DIGITAL CONVERTOR
DRAWN:D.NAIR
24 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 13

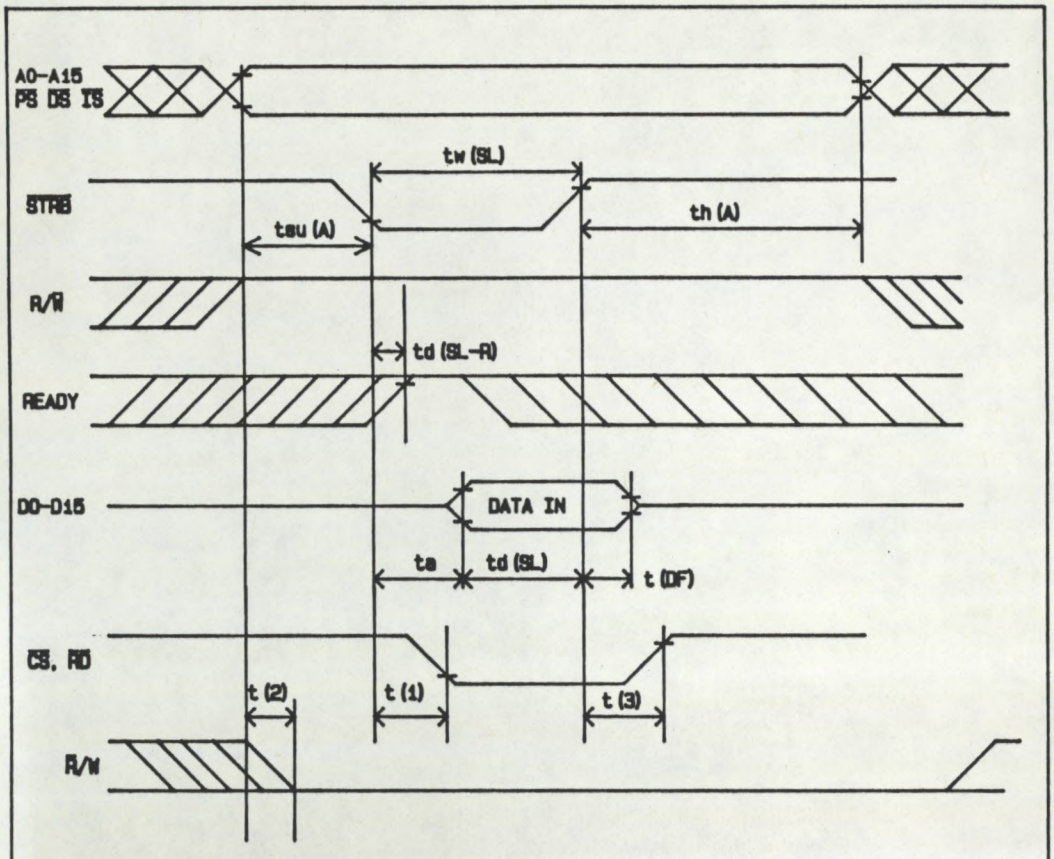
the multiplexer logic levels are different from the processor logic levels.

The analog multiplexer output is fed into a OP27, ultra low offset amplifier. This amplifier can be linked out of the system if required. If included in the signal path the gain of the amplifier can be selected by R36, and fine tuned by R49. This output is then fed into the sample and hold.

4.3 Read Timing (Refer to Figure 14.)

The A/D converter is mapped in the I/O space at port 0.
13 ns after /STRB goes low the decoder is enabled. After a time delay of 10 ns [t(PHL)74AS138]the output of the I/O space decoder is valid. Data is valid after 90 ns. [t(a) = 90 ns]. Because 40 ns < t(a) < 140 ns one wait state is needed. This is alredy implemented since all devices in the I/O space are accessed using one wait state. Ready is valid in the next cycle and the processor begins terminating the access. Data is clocked into the TMS320C25 on the rising edge of the /STRB signal. 10 ns after /STRB goes high the MAX162 starts entering high impedance state. After a maximum time of t(DF) = 20 ns the A/D would enter high impedance state. The total disable time is 30 ns therefore bus conflict is avoided if a read cycle is followed by a write cycle.

FIGURE 14. READ CYCLE TIMING OF AD7572/MAX162 (ONE WAIT STATE)



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	105ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	100ns (max)
Address Hold Time	th (A)	17ns (min)
Data Setup Time	td (SL)	127ns (max)
Data Disable Time	t (DF)	20ns (max)
Propogation Delay -74AS138	t (1), t (3)	10ns (max)
Propogation Delay -74AS04	t (2)	4ns (max)
Access Time of AD7572/MAX162	t (a)	90ns (typ)

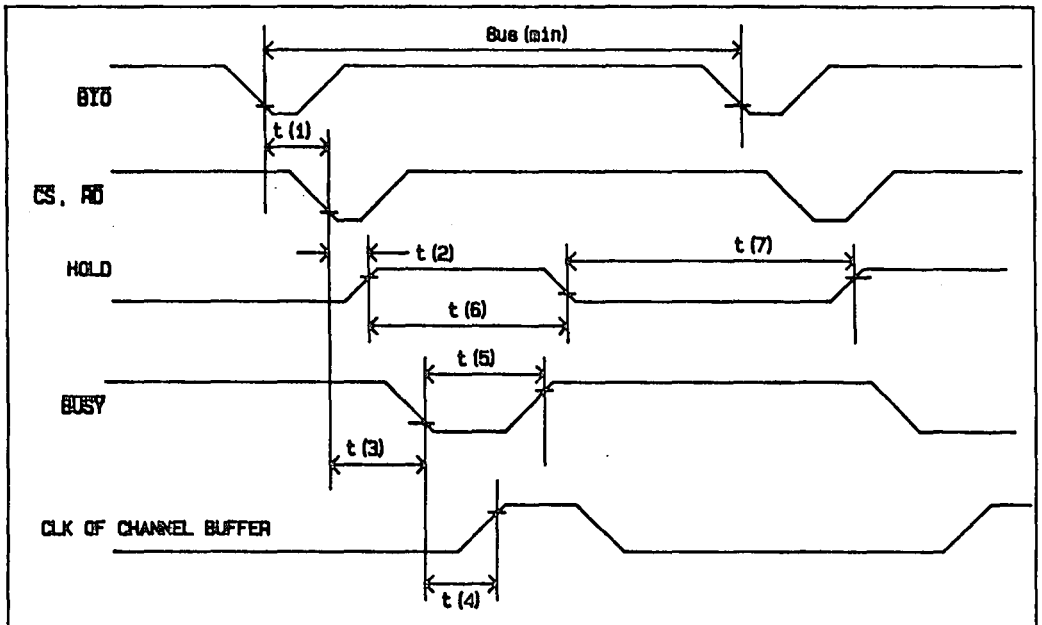
4.4 Data Acquisition Timing (Refer to Figure 15 and 16).

The two areas of timing that are crucial to device operation and accuracy are the A/D read operation and the settling times of the analog multiplexer and sample and hold respectively.

The maximum sample frequency of the system A/D converter is 125KHz. A free running baud rate generator chip is used to generate the various sample frequencies. The required sample frequency is selected using links and switch X7.

At a maximum sample frequency of 125KHz, the time between samples would be 8us. Refer to timing diagram in Fiqure 15 and 16. When the processor requires a particular channel to be digitised, the default channel number must be written at output port 1. A time of 3us must be allowed for the multiplexer to settle to the input value. This is only neccessary for the first conversion. A start of conversion is initiated by a read of the A/D buffer. Therefore the first value is read and "thrown away". This read would have been performed after 8us with the A/D sampling at its maximum rate of 125 KHz. A flip-flop is used to advance the HOLD signal to sample and hold because it has a settling time that is longer than the time the A/D takes to make the decision whether to set or drop the MSB(DB11). This time is effectively tuned out by generating the HOLD command using the I/O port select of the A/D. HOLD is therefore asserted after a time delay 35ns [t(2)]. After 250 ns [t(3)] /BUSY is asserted. 230 ns [t(5)] after /BUSY goes low the MSB decision is made. Therefore the total time that is allowed for the AD585 to settle is t(3) + t(5) $\leq$ 250 ns + 230

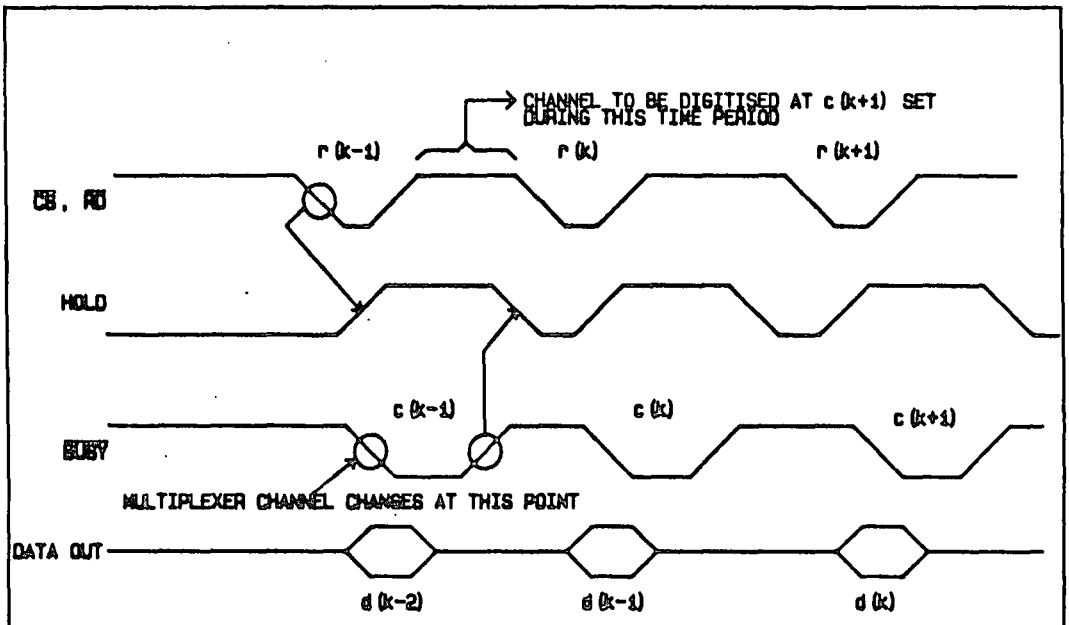
FIGURE 15. TIMING OF SAMPLE-AND-HOLD, ANALOG-TO-DIGITAL CONVERTER AND ANALOG MULTIPLEXER



* Denotes value of time dependant on software.

SIGNAL DESCRIPTION	SYMBOL USED	VALUE
$\overline{BIO}$ Active to A-D Read	t (1)	*
$\overline{CS}$ of A-D to HOLD Active	t (2)	35ns (max)
$\overline{CS}$ of A-D to $\overline{BUSY}$ Active	t (3)	230ns (min)
$\overline{BUSY}$ active to CLK of Channel		
Select Buffer	t (4)	5ns (max)
A-D Conversion Time	t (5)	5us (max)
HOLD Mode Duration	t (6)	5, 3us (max)
Minimum Acquisition Time of		
Sample-and-Hold (AD585)	t (7)	3us

FIGURE 16. RELATIONSHIP BETWEEN CONVERSION, CHANNEL NUMBER AND DATA READ.



r (k) = Read at Time = 0
c (k) = Conversion Initiated at Time = 0
d (k) = Data for conversion at c (k)

CHANNEL SELECTION: The channel whose data is required at c (k) must be written out to channel selection buffer before event r (k-1).

ns = 480 ns which is approximately equal to 500ns. The rising edge of the /BUSY signal is used to clock a logic 1 into the flip-flop and remove the HOLD signal from the sample and hold, placing it into the track mode. The select signal of the A/D is used to clear the flip-flop and place the sample hold in the track mode.

The timing relating to the analog multiplexer is critical because the channel can only be changed once the sample and hold is truly in the hold mode. A description of this timing follows. The channel number of the next channel to be acquired is written after a read of the A/D is performed. The AD585 has aperture time of 35ns. t(2) is the time that HOLD command is active after a read is performed from the MAX162. Therefore after a maximum time 70ns after the read the AD585s input is guaranteed to be isolated from the HOLD capacitor. After t(3) = 230ns /BUSY is active. The busy signal is inverted and the rising edge of this signal is used to clock the next channel number to the address select inputs of the analog multiplexer. The channel number is therefore only changed after a minimum time of 230ns - 70ns = 160ns after the sample and hold is truly in the HOLD mode. Changing the channel while the A/D is busy doing a conversion gives the analog multiplexer 8us -3us = 5us to settle to the new channel voltage. This is 2000ns more than the 3000ns required to achieve an accuracy of 0.01% at the output of the multiplexer.

4.5 Range Selection

The input range of the A/D converter is 0 to 5V. In order to implement an A/D converter with bipolar ranges an, op-amp is required to offset the analog input voltage. The op-amp at the input of the AD585 sample and hold is used to offset the input voltage. The output codes from the A/D converter is therefore offset binary. The equations expressing the output voltage as a function of resistor values is given below:

$$V(out) = [\ 1{,}48 \times V(in)\{Rx/(Ry + Rx)\} + 2{,}5V]$$

where Rx = [R22+R41]; [R33+R42]; [R34+R44]

and Ry = R26

The resistor values are calculated for the following ranges:

$$-2{,}5\ V < V(in) < +2{,}5\ V$$
$$-5\ V < V(in) < +5\ V$$
$$-10\ V < V(in) < +10\ V$$

The required range is selected by inserting and removing the appropriate links as indicated by the A/D range selection table as indicated below.

TABLE 2

Range	L26	L58	L59
-2,5V < V(in) < +2,5V	IN	OUT	OUT
-5V < V(in) < +5V	OUT	IN	OUT
-10V < V(IN) < +10V	OUT	OUT	IN

4.6 Calibration

Offset is adjusted before full scale. 1/2 LSB is applied to the analog input and R47 are adjusted until the output code flickers between 8000(HEX) and 8010(HEX). This sets the zero point.

Full scale voltage is set by applying a full scale voltage less 3/2LSB to the analog input. R41, R42 or R44 is adjusted until the output code flickers between FFE0(HEX) and FFF0(HEX).

The above function can be performed using the emulator or by running a test program.

CHAPTER 5

5.0 DIGITAL-TO-ANALOG CONVERTER

During development it is necessary to output processed data in analog form. This is accomplished by a digital-to-analog converter. The converter selected is the ANALOG DEVICES AD767. The AD767 is a 12 bit D/A converter. The device has an on-chip output amplifier, high stability buried zener reference and a fast 12 bit parallel data latch requiring 40 ns write pulse width. These features reduce the number of external components required.

The settling time of the D/A converter is 3 us and is suitable for this application because data will never be output faster than the digitisation process which in this design will not exceed the maximum sampling frequency which is limited to 125 KHz. The time delay between samples has to be a minimum of 6 us to allow for the output of the D/A and the analog multiplexer to settle. The D/A and the multiplexer both have a maximum settling times specified at 3us. Capacitors to store the analog voltage have to be implemented in external circuitry in addition to de-glitching circuitry. An output multiplexer is implemented in the D/A section giving the system the capability to output 8 analog signals. Another multiplexer is used as a feedback multiplexer and fed into a negative feedback amplifier to compensate for voltage errors in the output path.

5.1 Channel Selection and Output of Data

Both the channel number and the digital data to be output are mapped to the same address. The digital data to be output is ANDED with channel number and then output at I/O PORT location 5. The address of the channel forms the lower 3 bits (DB0-DB2) of the word to be written at port address 5. The upper 12 bits (DB4-DB15) comprise the data to be output to the D/A. This scheme makes efficient use of code because channel selection and the output of data is accomplished in single instruction.

5.2 Write Cycle Timing (Refer to Fiqure 18 and 19)

The I/O space decoder is enabled by the /STRB signal. Therefore after a time = t(PHL)74AS138 = 10ns the I/O port signal is valid. The data setup time before /IOPRT5 goes high is 132 ns. The required data setup time for the AD767 is t(DS) = 40 ns. This requirement is satisfied because t(su) is much greater than t(DS). The rising edge of /IOPRT5 clocks data into the latch of the AD767. Note that all devices in the I/O space are accessed with one wait state. Although it is not required for this particular access, it made READY signal generation simpler.

The other device written to in the same cycle is the channel selection register. The register is also selected by /IOPRT5 going low. The data setup time t(su) = 132 ns which is greater than the 10 ns mimimum setup time required by 74AHCT374.

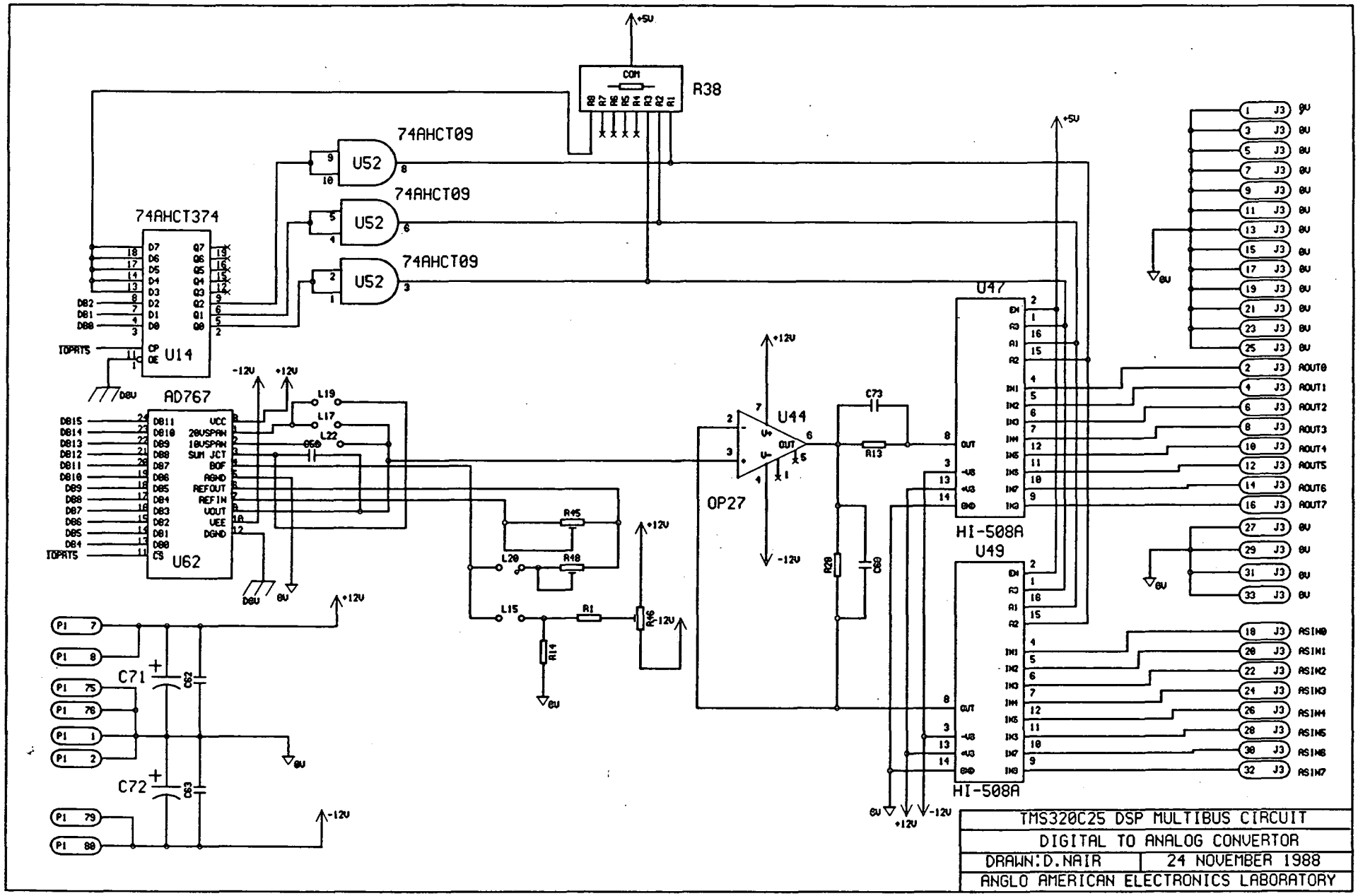
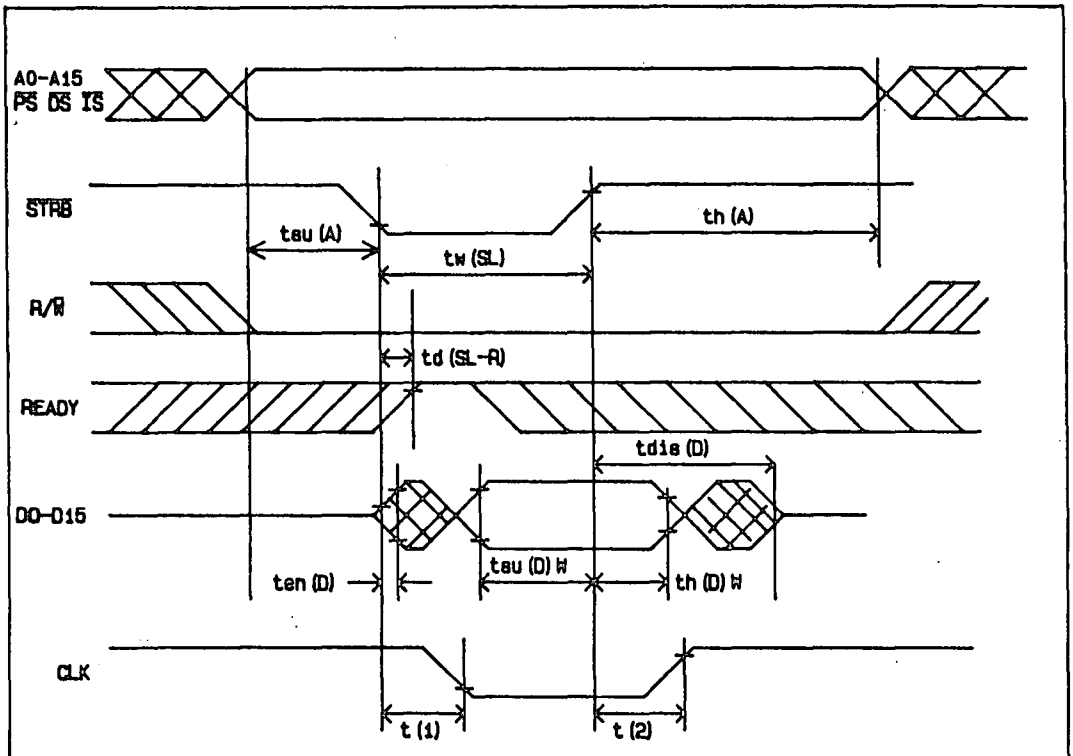

+5U
COM
R38
74AHCT09
U52
74AHCT374
U14
IOPRTS
AD767
U62
-12U
+12U
L19
L17
L22
C60
R45
L20
R48
L15
R1
R14
R46
C71
C72
C62
C63
P1 7
P1 8
P1 75
P1 76
P1 1
P1 2
P1 79
P1 80
U44
OP27
C73
R13
R28
C80
U47
U49
HI-508A
J3
AOUT0
AOUT1
AOUT2
AOUT3
AOUT4
AOUT5
AOUT6
AOUT7
ASIN0
ASIN1
ASIN2
ASIN3
ASIN4
ASIN5
ASIN6
ASIN7
TMS320C25 DSP MULTIBUS CIRCUIT
DIGITAL TO ANALOG CONVERTOR
DRAWN:D.NAIR
24 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

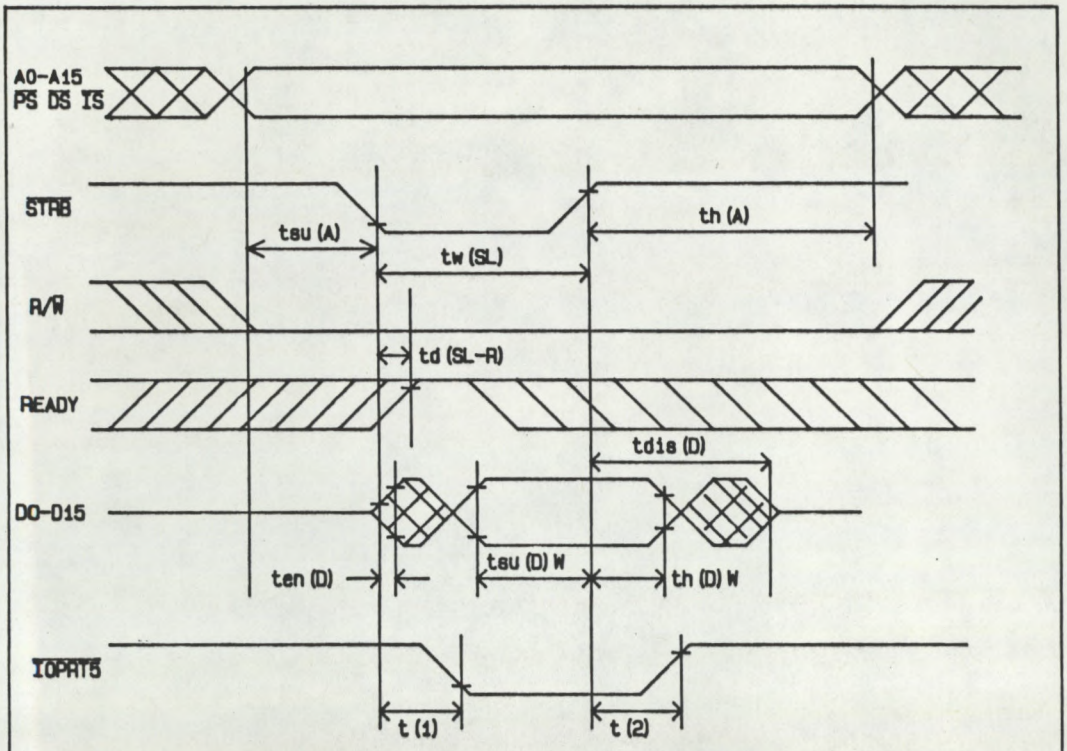
FIGURE 17

FIGURE 18. WRITE CYCLE TIMING FOR 74AHCT374
(ONE WAIT STATE)



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	105ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	150ns (max)
Address Hold Time	th (A)	17ns (min)
Data Bus Drive Time	ten (D)	15ns (min)
Data Bus Write Setup Time	tsu (D) W	138ns (max)
Data Write Hold Time	th (D) W	15ns (min)
Data Bus Disable Time	tdis (D)	40ns (min)
Propogation Delay -74AS138	t (1), t (2)	10ns (max)

FIGURE 19. WRITE CYCLE TIMING FOR AD767
(ONE WAIT STATE)



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	105ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	150ns (max)
Address Hold Time	th (A)	17ns (min)
Data Bus Drive Time	ten (D)	15ns (min)
Data Bus Write Setup Time	tsu (D) W	138ns (max)
Data Write Hold Time	th (D) W	15ns (min)
Data Bus Disable Time	tdis (D)	40ns (min)
Propogation Delay -74AS138	t (1), t (2)	10ns (max)

The output of the 74AHCT374 is pulled low so that the channel is changed as soon as the data at the output is valid. The output drives a 74AHCT09 open drain AND gate configured as a buffer to perform level shifting neccessary because of the different logic levels between the multiplexer and the processor.

5.3 Range Selection (Refer to Table 3).

The outputs and sense inputs is available at connecter J3. All ground (0V) connections are on the component side. The ranges available are bipolar and unipolar and are selected as per link table.

The ranges available are:

-10V < V(out) < +10V

-5V < V(out) < +5V

-2,5V < V(out) < +2,5V

0V < V(out) < +5V

0V < V(out) < +10V

5.4 Calibration

For this to be performed a simple test program has to written or an in-circuit emulator can be used.

Unipolar Configuration

Select the unipolar range as required.

DIGITAL-TO-ANALOG CONVERTER RANGE SELECTION TABLE

	BIPOLAR			UNIPOLAR	
LINK NAME	+/-10V	+/-5V	+/-2,5V	0-5V	0-10V
L20	IN	IN	IN	OUT	OUT
L15	OUT	OUT	OUT	IN	IN
L17	IN	IN	IN	OUT	IN
L22	OUT	IN	IN	IN	IN
L19	OUT	OUT	OUT	OUT	OUT

TABLE 3

STEP 1 ...ZERO ADJUST

All bits are turned OFF and zero trimmer R46 is adjusted until the output reads 0.000 volts. (1 LSB = 2,44 mV).

STEP 2 ...GAIN ADJUST

All bits are turned ON and gain trimmer R45 is adjusted until the output is adjusted to 1 LSB (2,44 mV) less than nominal full scale voltage.

Bipolar Configuration

Select the bipolar range as required. Positive full scale occurs with all the bits ON.

STEP 1 ...OFFSET ADJUST

All bits are turned OFF. R48 is adjusted to give the mimimum voltage at the output, correct to three decimal places.

STEP 2 ...GAIN ADJUST

All bits are turned ON. R45 is adjusted to give a reading that is 2,4 mV less than the full scale voltage.

STEP 3 ...BIPOLAR ZERO ADJUST

If an accurate zero output is required, the MSB is set ON and all other bits OFF. R48 is readjusted for zero volts output.]

CHAPTER 6

6.0 SAMPLE RATE GENERATOR

There are three methods that can be used to generate various sample rates for the A-D converter using the TMS320C25:

a) Timer interrupt
b) Fixed clock generator tied to /BIO pin.
c) End-of-conversion driving either the /BIO or one of the interrupt signals.

a) Timer interrupt(TINT): The TMS320C25 has an on chip timer that can be programmed to generate a wide range of sample frequencies. This is under software control. The timer is loaded with a 16 bit value, and is decremented at the frequency of CLKOUT1. When the count reaches zero a timer interrupt (TINT) is generated. In the next cycle the contents of the period (PRD) register are loaded into the timer (TIM) register. By programming the PRD register from 1 to 65535 a TINT can be generated every 2 to 65535 cycles of CLKOUT1 respectively. The interrupt frequency is given by the equation below:

F = FREQUENCY OF CLKOUT1/(PRD+1)

Therefore the sample rate range is given by:

5 MHz < F < 152,58 Hz

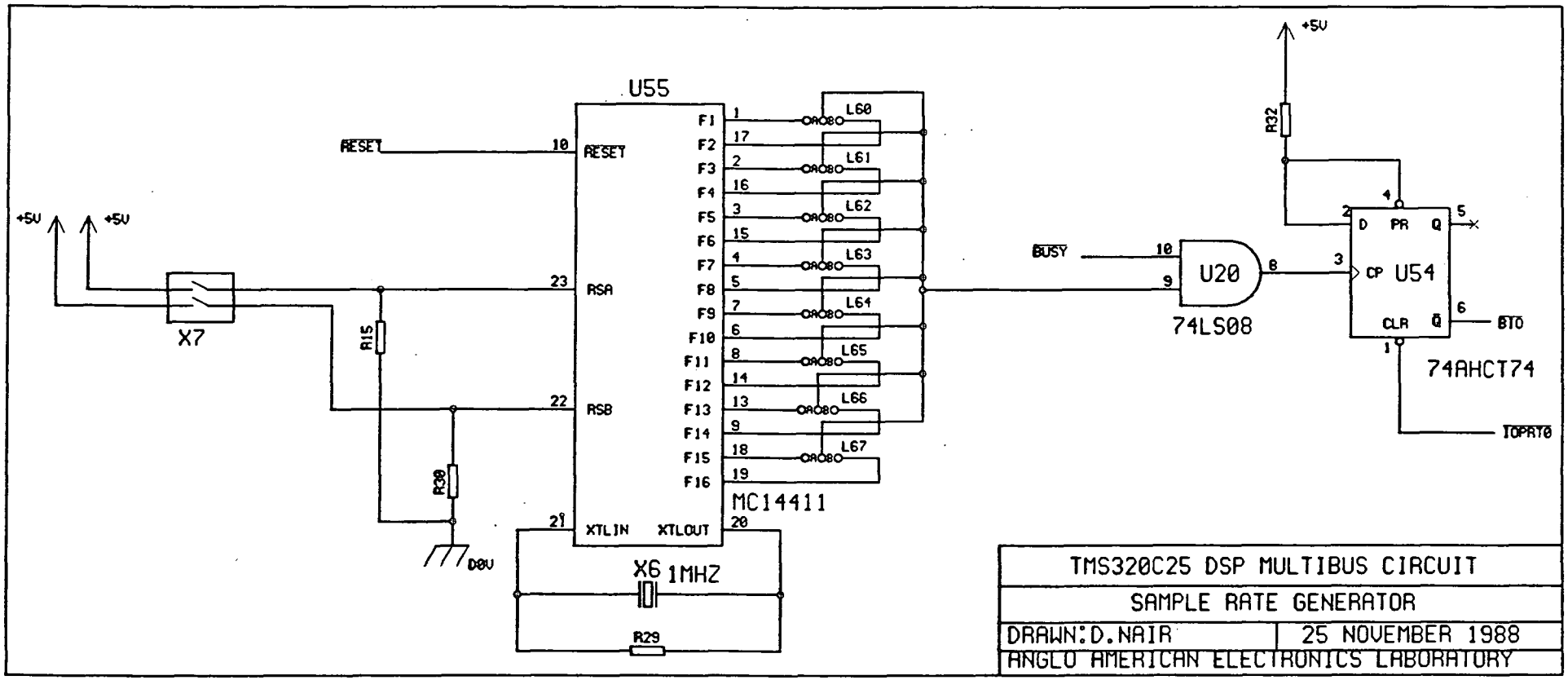

U55
RESET
RESET
RSA
RSB
XTLIN
XTLOUT
MC14411
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
F16
L60
L61
L62
L63
L64
L65
L66
L67
+5V
+5V
X7
R15
R30
D0V
X6 1MHZ
R29
BUSY
U20
74LS08
R32
U54
D
PR
Q
CP
CLR
Q̄
74AHCT74
BTO
IOPRT0
TMS320C25 DSP MULTIBUS CIRCUIT
SAMPLE RATE GENERATOR
DRAWN: D.NAIR
25 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 20

The advantage of using this method is that power down mode of processor can be used and a wide range of sample rate frequencies are available. A change in sample rate frequencies requires a software change.

b) Fixed clock generator tied to the /BIO pin: This method has been designed into the system because it allows sample rates to be changed without any need for software change. In this method the /BIO pin can be polled continuously or in certain sections of the program.

The sample rate frequencies are generated using a MC14411 bit rate generator. Refer to Fiqure 20. The output of the bit rate generator is fed into a D type flip-flop. The data input to the flip-flop is tied to the /BUSY signal from the A-D converter. This prevents /BIO from going low during an A-D conversion. So on a rising edge of the clock output from the bit rate generator /Q goes low pulling /BIO low also. /Q is reset high when the read of the A-D is done. The next rising edge of the output from the bit rate generator will send /Q low provided that /BUSY is high.

The various sample rates are shown in the Table 4 and the sample rate is selected by inserting the link in the appropriate position.

c) Fixed clock generator tied to an interrupt signal: The TMS320C25 has three interrupt signals. /INT0 is used for Multibus communications and /INT3 is used for the

SAMPLE RATE FREQUENCY SELECTION

RATE SELECT

X7(1)	X7(2)	RATE
OFF	OFF	X1
OFF	ON	X8
ON	OFF	X16
ON	ON	X64

ALL VALUES ARE IN THE UNIT HERTZ

OUPUT	LINK	X64	X16	X8	X1
F1	L60A	333K	83K	41K	5,2K
F2	L60B	250K	62,5K	31,2K	3,9K
F3	L61A	166K	41,6K	20,8K	2,6K
F4	L61B	125K	31,2K	15,6K	1,9K
F5	L62A	83,3K	20,8K	10,4K	1,3K
F6	L62B	62,5K	15,6K	7,8K	976
F7	L63A	41,6K	10,4K	5,2K	651
F8	L63B	20,8K	5,2K	2,6K	325
F9	L64A	10,4K	2,6K	1,3K	162
F10	L64B	6,9K	1,7K	865	108
F11	L65A	5,2K	1,3K	651	81
F12	L65B	4,6K	1,1K	584	73
F13	L66A	3,9K	995	497	62
F14	L66B	2,6K	650	325	40
F15	L67A	100K	500K	500K	500K
F16	L67B	1M	1M	1M	1M

TABLE 4

pushbutton interface. It was decided that /INT2 should be reserved and it was therefore not used in the design of the sample rate generator.

CHAPTER 7

7.0 RESET GENERATOR TIMING AND WATCHDOG

The reset generator and watchdog are built around the Texas Instruments TL7705A supply voltage supervisor chip. The supply voltage supervisor resets the microprocessor system during power up and supply voltage dropout.

7.1 The Supply Voltage Supervisor

Any TTL based design requires that the supply voltage remain above 4,77V for reliable operation. Below this level logic levels cannot be guaranteed. In a microprocessor system such a fault can lead to program failure even if the supply voltage dip is only for a short duration.

To provide a smooth restart after such a dip, a reset pulse is required. The TL7705A provides this function by constantly monitoring its supply voltage and if its drops below 4,77V generates a controlled width reset pulse. Refer to timing diagram in Fiqure 22.

The reset pulse width is given by t(d) = 1,3 x 10exp4 x C(t)
For a reset pulse width of 200 ms a capacitance of 22uF is required. Supply voltage glitch capture is of 1us. A reset pulse is also generated if the push button is depressed or if the multibus "INIT" (initialise slave) signal goes low.

7.2 Watchdog (Refer to Fiqures 21 and 23)

The TL7705A has a RESIN input. Pulling this input low generates a reset pulse. A capacitor is connected to the RESIN input. Watchdog pulses from the XF pin of the TMS320C25 constantly recharge this capacitor keeping the RESIN input at logic 1 level. These pulses are under software control.

If pulses fail due to microprocessor error, the capacitor C2 discharges via resistor R8. When RESIN drops below its threshold, a fixed period system reset pulse is generated.
The watchdog circuit is also reset with C2 being recharged from reset pin 6 output via X2 and R50. If watchdog pulses do not restart, capacitor X2 goes through alternating discharge and recharge cycles opeerating as an astable continually issuing RESET pulses.

During refresh pulses C2 charges via X3 and C59. (Refer to timing diagram. When the refresh signal goes low C2 starts to discharge via R8. In normal operation discharge is ideally from 4,0V to 2,3V at the RESIN input. With a refresh pulse rate of 1KHz and a 10% duty cycle , a R8,C2 time constant of 1,6ms is required. Due to the bias current of the RESIN input the value of R8 must be limited to keep the RESIN below its threshold. Allowing for a bias current of 5uA gives R8 a value of 75K with a voltage at RESIN at 0,375V. C2 is thus calculated to be 22nF. This results in a reset pulse being generated whenever three or more refresh

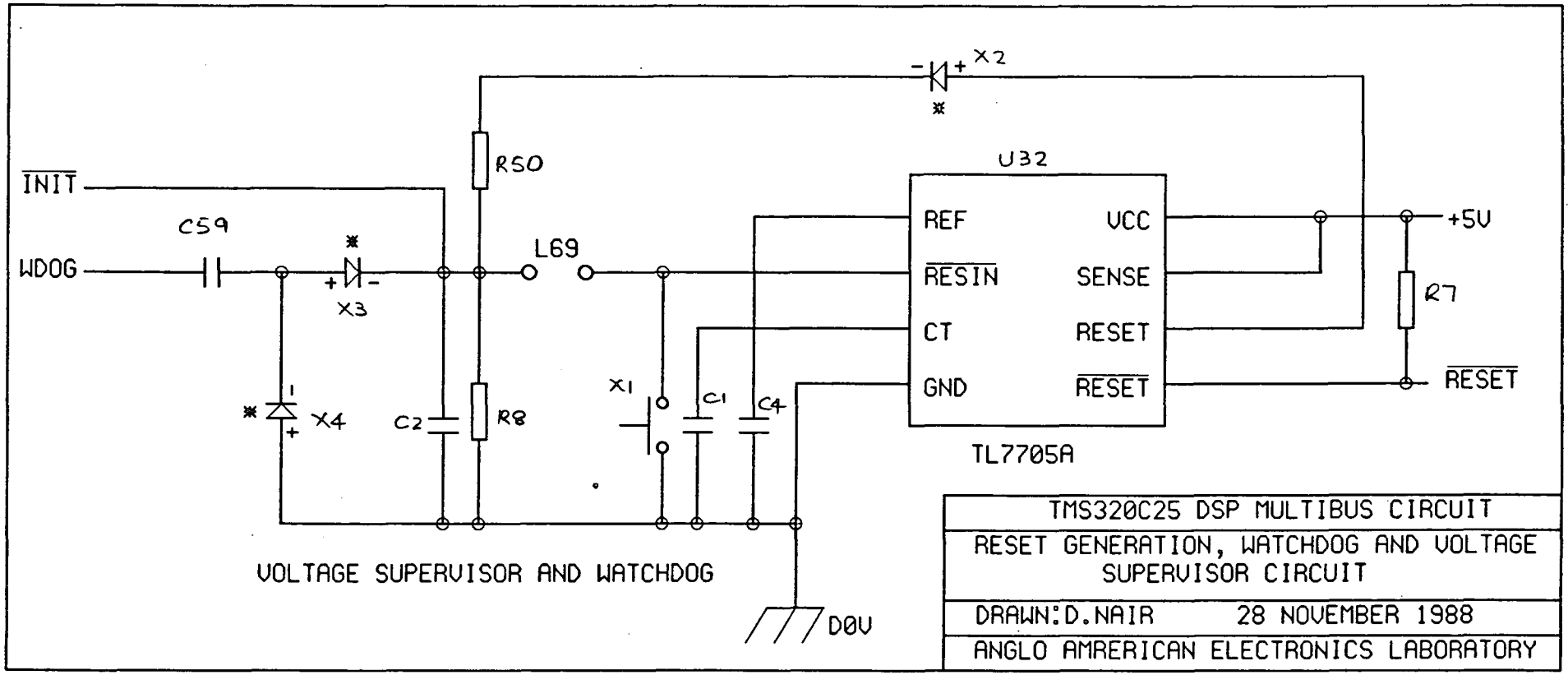
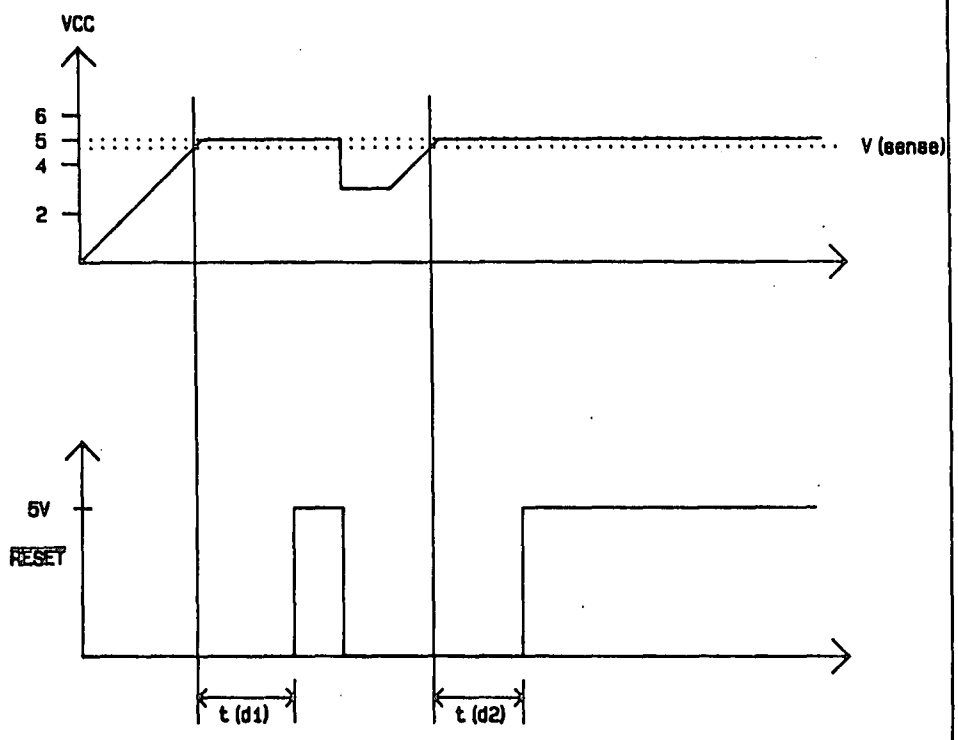

X2
R50
U32
INIT
C59
WDOG
L69
REF
VCC
+5V
RESIN
SENSE
X3
R7
CT
RESET
X1
C1
C4
GND
RESET
X4
C2
R8
TL7705A
VOLTAGE SUPERVISOR AND WATCHDOG
D0V
TMS320C25 DSP MULTIBUS CIRCUIT
RESET GENERATION, WATCHDOG AND VOLTAGE SUPERVISOR CIRCUIT
DRAWN: D.NAIR 28 NOVEMBER 1988
ANGLO AMRERICAN ELECTRONICS LABORATORY

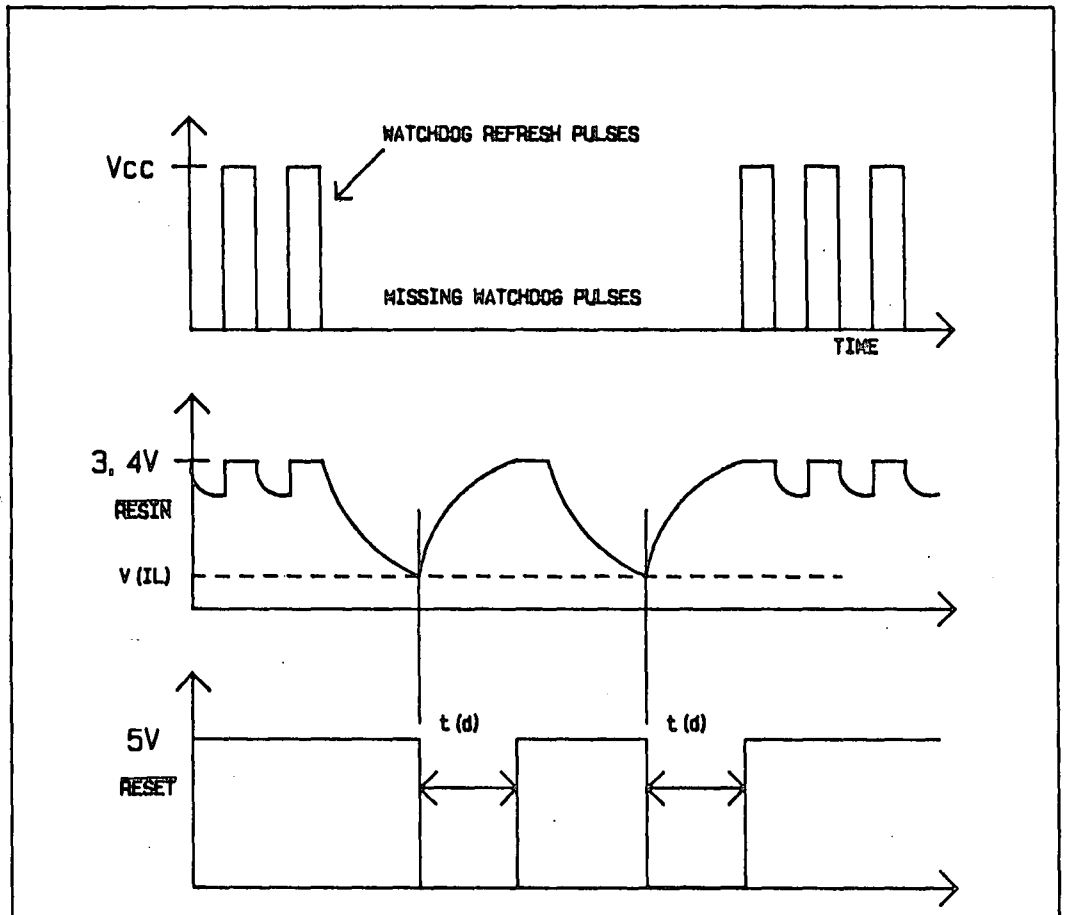
FIGURE 21

FIGURE 22. POWER UP AND DROP OUT RESET TIMING



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Power up reset	t (d1)	200ms
Drop out reset	t (d2)	200ms

FIGURE 23. WATCHDOG TIMING



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Reset pulse width	t(d)	200ms

pulses are missing. The R8,C2 time constant decides the period between reset pulses.

CHAPTER 8

8.0 MULTIBUS INTERFACE

8.1 Multibus Transfer of Word from TMS320C25

The multibus latches are mapped into the I/O space and its address is /IOPRT4. A transfer is performed by a write to the latches at this address using the OUT instruction; eg.

```
OUT DATA,PA4
```

Data is written using one wait state. The timing diagram is the same as the analog multiplexer channel selection, that is for the 74AHCT374. Note that a single transfer of data also generates the neccessary interrupt to the multibus master. This interrupt is automatically cleared once the master performs a read of the high byte. An active low signal on initialse (/INIT) also clears the interrupt. The rising edge of the /IOPRT4 signal clocks the flip-flop at U19. /Q output goes low. This signal is tied to interrupt levels /INT0-/INT7 on the multibus bus. The required interrupt level is selected by inserting the neccessary link as indicated by Table 5.

The ability to select one of 8 interrupt levels gives the capability to use up to 8 TMS320C25 processor boards to be used concurrently.

8.1.1 Master Read of Slave

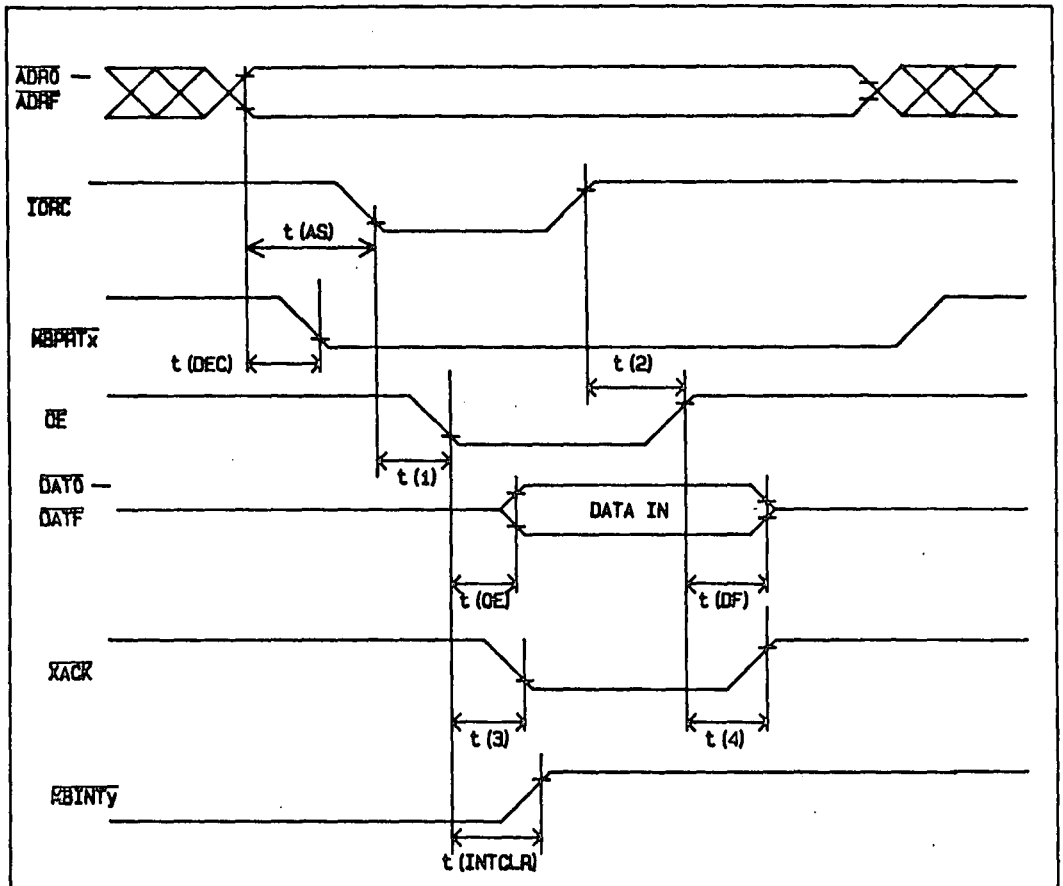
The latches on the slave board are configured for a master based on an eight bit microprocessor. This means that a read of 16 bit data has to be performed in two cycles. Therefore the two latches U11 and U12 are mapped into two different port addresses of the multibus address range. In response to an interrupt generated by the slave, the master must first read the low byte at /MBPRT2. The high byte must then be read at /MBPRT3. During this second cycle the multibus interrupt is automatically cleared. This would complete the transfer of the word from the TMS320C25 to the master.

8.1.2 Timing Information (Refer to Figures 24 and 27)

On receiving an interrupt from the DSP board after a data transfer, the master would respond by accessing the latches U11 and U12. The description of the timing associated with this transfer assumes that the master is in the software cycle to transfer data from the DSP board to the master.

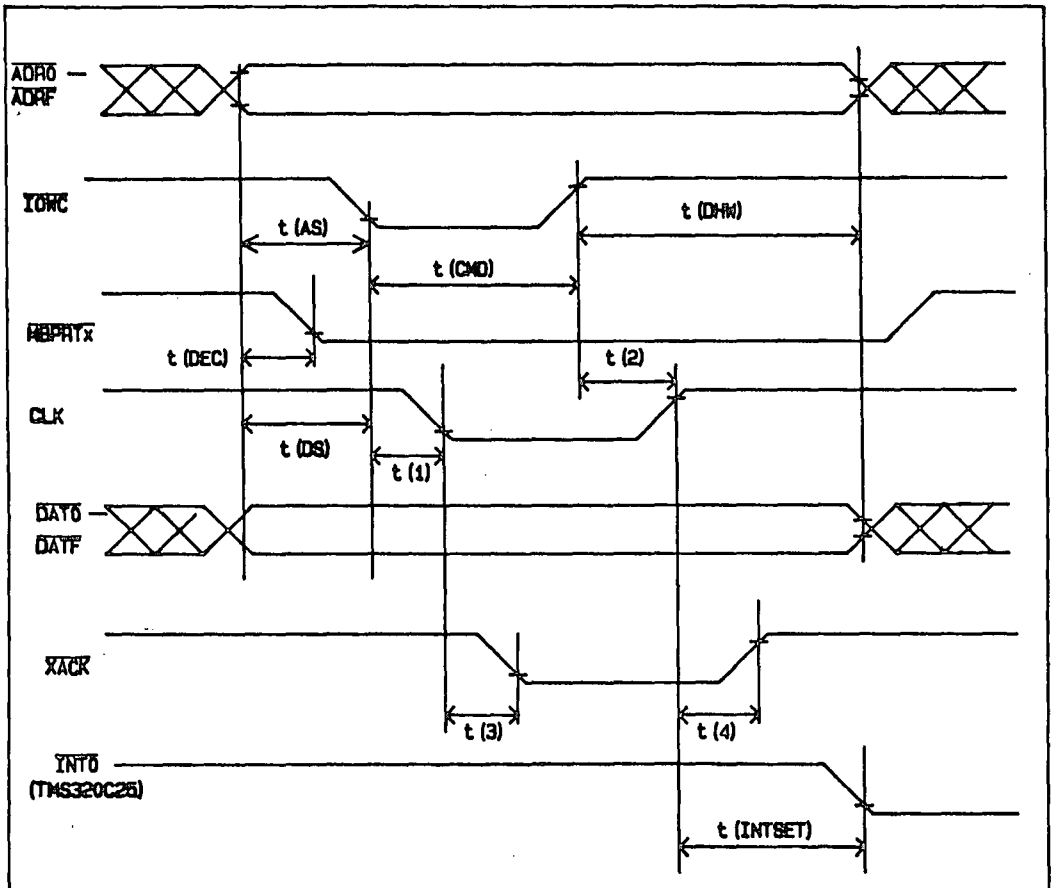
After a minimum time address setup time of 50 ns [t(AS)], /IORC goes low indicating that an I/O read cycle is in progress. /MBPRT2 goes low after a maximum time of 40 ns [t(DEC) = 2 x t(PHL)74AHCT138 = 40 ns]. 5,8ns after /IORC goes low, /OE of the 74AHCT374 goes low. 23 ns [t(OE)] later data output from the 74AHCT374 is valid. Data is therefore valid 51.6 ns after /IORC goes low. This is much less than the 100ns data setup time required by the multibus timing before /IORC goes high again.

FIGURE 24. MULTIBUS READ CYCLE TIMING



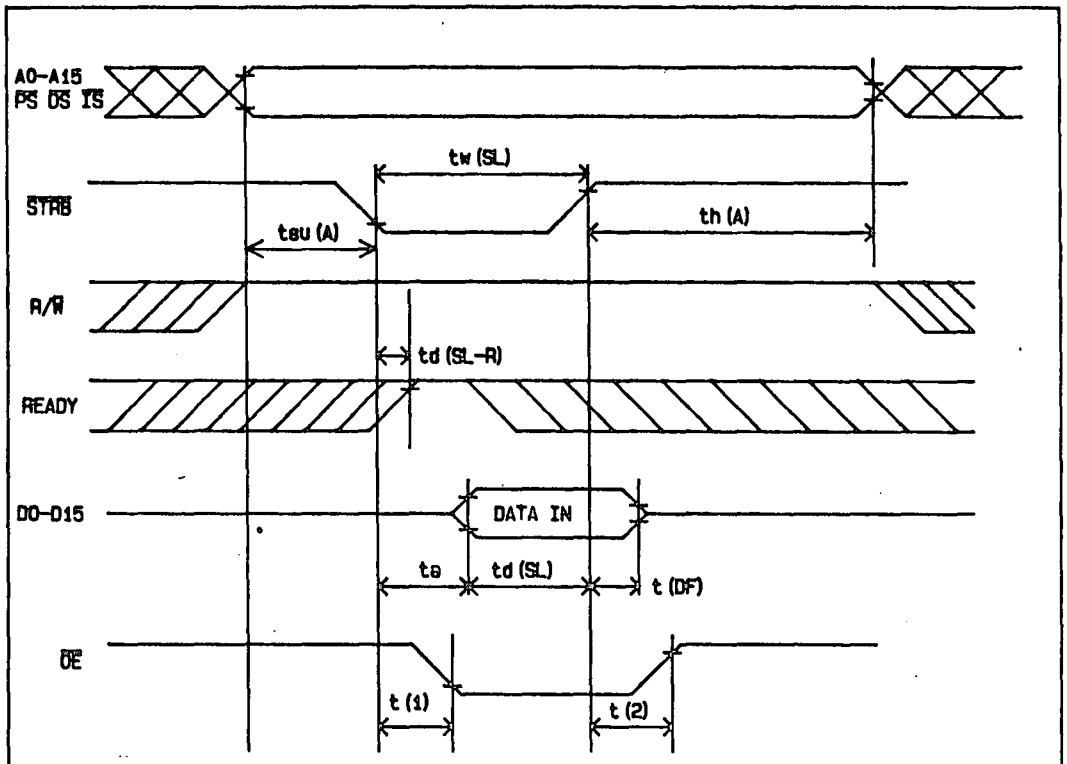
SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	t (AS)	50ns (max)
Address Decoding Delay	t (DEC)	40ns (max)
Propogation Delay -74AS32	t (1)	5, 8ns (max)
Propogation Delay -74AS32	t (2)	5, 8ns (max)
Output Enable to Interrupt		
Clear	t (INTCLR)	15ns (max)
$\overline{OE}$ to Data Valid	t (OE)	27ns (max)
$\overline{OE}$ Low to $\overline{XACK}$ Low	t (3)	15ns (max)
$\overline{OE}$ High to $\overline{XACK}$ High	t (4)	15ns (max)
$\overline{OE}$ High to Data Float	t (DF)	18ns (max)

FIGURE 25. MULTIBUS WRITE CYCLE TIMING



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	t (AS)	50ns (max)
Address Decoding Delay	t (DEC)	40ns (max)
Propogation Delay -74AS32	t (1)	5, 8ns (max)
Propogation Delay -74AS32	t (2)	5, 8ns (max)
Data Setup Time	t (DS)	50ns (max)
Write Pulse Width	t (CMD)	100ns (max)
CLK High to Interrupt Set	t (INTSET)	35ns (max)
CLK Low to $\overline{\text{XACK}}$ Low	t (3)	15ns (max)
CLK High to $\overline{\text{XACK}}$ High	t (4)	15ns (max)
Write Data Hold Time	t (DHW)	50ns (max)

FIGURE 26. READ CYCLE TIMING OF 74AHCT374
(ONE WAIT STATE)



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	105ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	100ns (max)
Address Hold Time	th (A)	17ns (min)
Data Setup Time	td (SL)	127ns (max)
Data Disable Time	t (DF)	18ns (max)
Propogation Delay -74AS138	t (1)	10ns (max)
Propogation Delay -74AS138	t (2)	10ns (max)
Access Time of 74AHCT374	t (a)	27ns (max)
Output Disable Time after		
$\overline{\text{STRB}}$ High	t (DF) +t (2)	28ns (max)
Data Valid After $\overline{\text{STRB}}$ High	t (1) +t (a)	33ns (max)

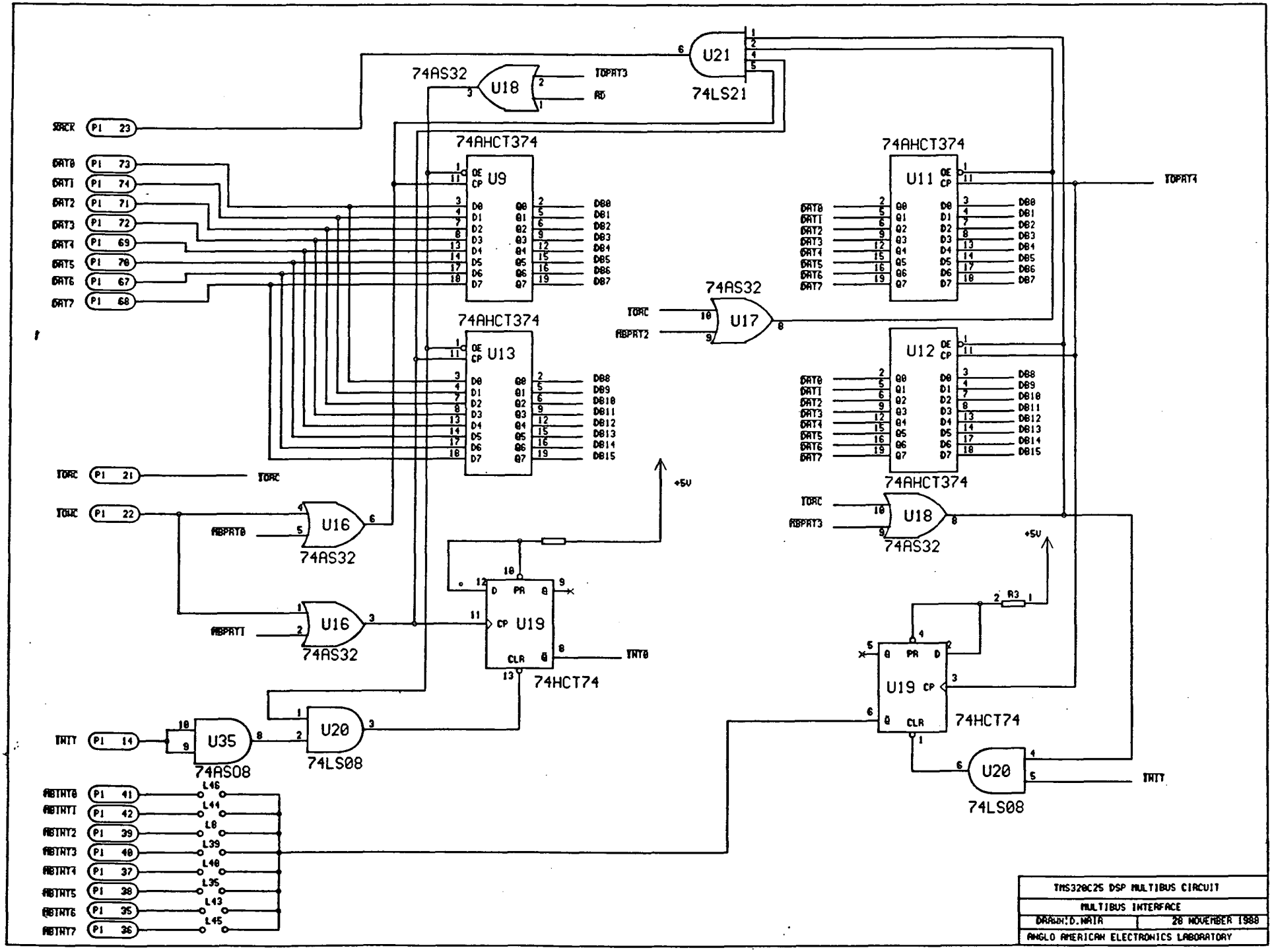

74AS32
U18
TOPRT3
RD
U21
74LS21
SRCK
P1 23
74AHCT374
U9
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
P1 73
P1 74
P1 71
P1 72
P1 69
P1 70
P1 67
P1 68
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
74AHCT374
U11
TOPRT4
74AS32
U17
TORC
ABPRT2
74AHCT374
U13
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
74AHCT374
U12
TORC
P1 21
TORC
TORC
P1 22
ABPRT0
U16
74AS32
ABPRT1
U16
74AS32
+5V
U19
74HCT74
INT0
R3
ABPRT3
U18
74AS32
U19
74HCT74
INTT
P1 14
U35
74AS08
U20
74LS08
U20
74LS08
ABINT0
ABINT1
ABINT2
ABINT3
ABINT4
ABINT5
ABINT6
ABINT7
P1 41
P1 42
P1 39
P1 40
P1 37
P1 38
P1 35
P1 36
L46
L44
L8
L39
L40
L35
L43
L45
TMS320C25 DSP MULTIBUS CIRCUIT
MULTIBUS INTERFACE
DRAWN:D.NAIR
28 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 27

Data is read at the rising edge of /IORC. This high transition disables the latches U11 and U12. The output of the latches enter high impedance state after a maximum time of 23,8 ns. [t(PLH)74AS32 = t(1) + t(DF)74AHCT374 = 5,8 ns + 18 ns]. Therefore t(DHR) = 23,8 ns which is much less than the 65ns maximum required by the multibus timing.

The tranfer acknowledge (/XACK) signal is driven by the select signals of both latches. This signal is fed into a four input AND gate and the output drives the /XACK signal directly. /XACK goes low after a maximum time of 20,8 ns [t(3) = t(PHL)74AS32 + t(PHL)74LS21 = 5,8 ns + 15 ns = 20,8 ns]. The minimum time after which /XACK can go low after /IORC low is 0 ns. This timing parameter is therefore met. 20,8 ns after /IORC goes high /XACK follows [t(4) = t(PLH)74AS32 + t(PLH)74LS21 = 5,8 ns + 15 ns = 20,8 ns]. This is much less than the maximum 65ns required for /XACK high after /IORC high.

The /OE signal of U12 is also used to clear the flip-flop at U19. The interrupt is cleared after a maximum time of 31,8 ns [t(PHL)74AS32 + t(PLH)74AHCT74 + t(PHL)74LS08 = 5,8 ns + 15 ns + 11 ns = 31,8 ns].

8.1.3 Multibus Address Decoding

The circuit diagram is shown in Figure 28 . The decoding scheme allows a maximum of 8 TMS320C25 boards to be operated in parallel with one master. Provision is made for 16 different addresses so that it may be used on the extended Multibus system. /ADR0,

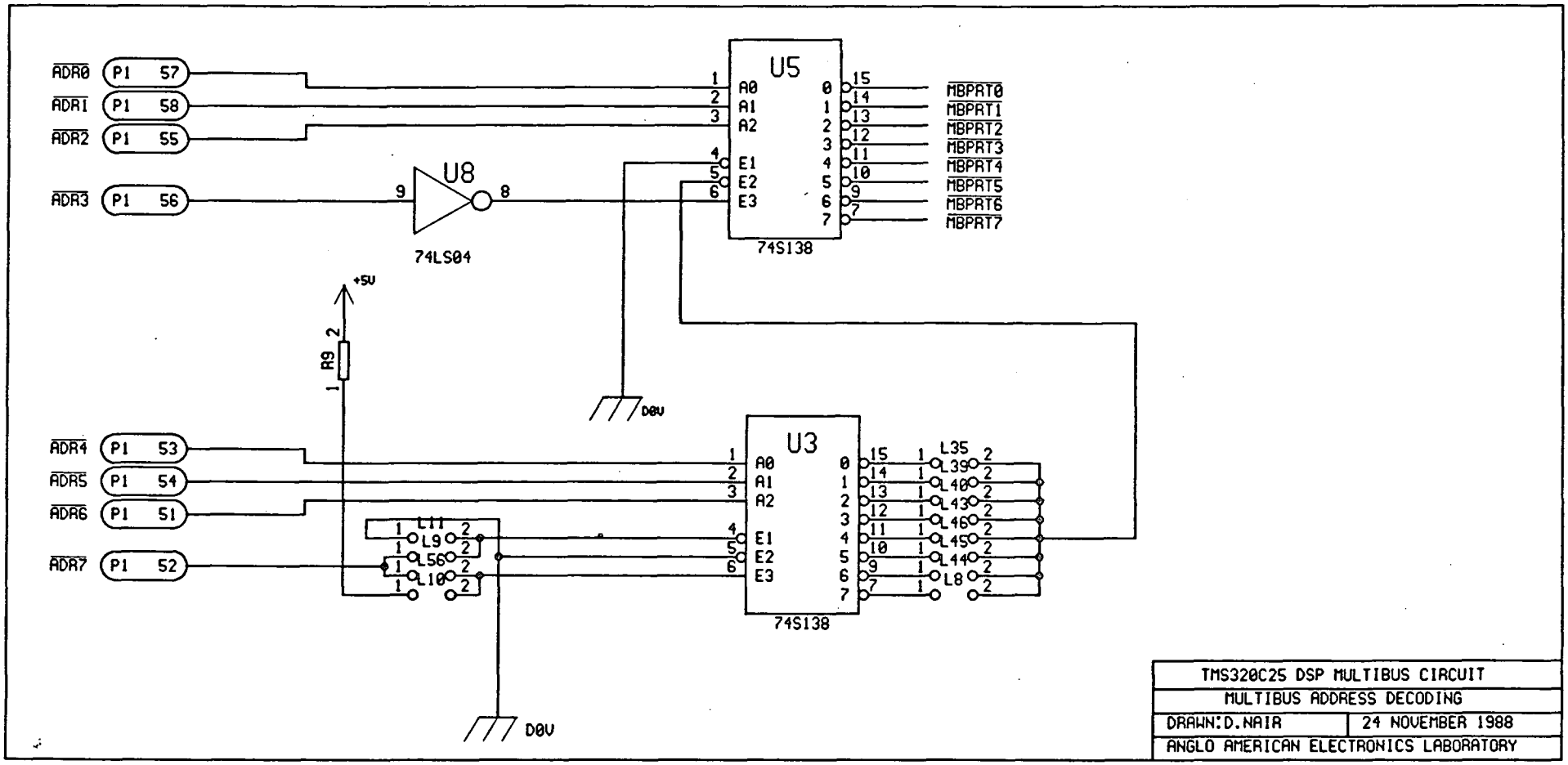

ADR0 P1 57
ADR1 P1 58
ADR2 P1 55
ADR3 P1 56
U8
74LS04
U5
A0
A1
A2
E1
E2
E3
74S138
MBPRT0
MBPRT1
MBPRT2
MBPRT3
MBPRT4
MBPRT5
MBPRT6
MBPRT7
+5V
R9
D0V
ADR4 P1 53
ADR5 P1 54
ADR6 P1 51
ADR7 P1 52
U3
L11
L9
L56
L10
L35
L39
L40
L43
L46
L45
L44
L8
TMS320C25 DSP MULTIBUS CIRCUIT
MULTIBUS ADDRESS DECODING
DRAWN: D.NAIR
24 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 28

/ADR1, /ADR2 control the address of the latches U9, U13, U12, U11. /ADR3 controls the enabling of decoder U5. /ADR3 must be low to enable the decoder U5. Valid addresses for the multibus latches are in the range 0 to 4 for the lower nibble of the address.

/ADR4, /ADR5, /ADR6 and /ADR7 control the board address. The appropriate links must be inserted as indicated by Table 6 for the board to be functional at the correct addresses.
Note that the address forms only the board address. The port addresses which is the lower nibble of the address byte must be concatenated with above board address so that the latches are selected as desired.

8.2 Multibus Transfer of Word to TMS320C25

The master transfers data to the TMS320C25 in a two byte transfer. The low byte is first written and then the high byte. The termination of the high byte write signal sets the TMS320C25 interrupt level 0(/INT0) active. Since the TMS320C25 has a 16 bit wide bus it can access the data in a single cycle. The two latches are U9 and U13. The multibus address for these two latches are 0 and 1 for the lower nibble. The upper nibble of the multibus address selects the board address. The TMS320C25 sees these latches at /IOPRT3.

8.2.1 Timing of Multibus Write

The timing is shown in Figure 25. /MBPRT(3,4) is valid after a maximum time of t(DEC)= 20ns. After a maximum address setup time of 50 ns [t(AS)]; /IOWC goes low indicating that an I/O write cycle is in progress. Data setup time t(DS)=50ns so that address and data are valid at about the same time. The CLK input of the latch goes low after maximum time of t(1) = 5,8 ns. Data at the input of the latch is valid for 100 ns before the rising edge of /IOWC signal. This is very much greater than the 14ns required by the 74AHCT374. The data hold time after /IOWC high is t(DHW) - 2 x t(PLH)74AHCT138 = 50ns - 20ns = 30ns. Data hold time for the 74AHCT374 after its CLK goes high is 0ns. This requirement is therefore met.

/XACK timing is the same as for multibus read of U11 and U12. /INT0 of the TMS320C25 is set on the rising edge of the CLK signal to U13. This is set after a maximum time of t(2) + t(INTSET) = 5,8ns + 35ns = 38,8ns; after /IOWC goes high.

8.2.2 Timing of TMS320C25 Read

Figure 26 shows the read cycle timing described below.
After a maximum address setup time of 13 ns [t(SU)], /STRB goes low. /IOPRT3 goes low after a maximum time of 10 ns [t(1) = t(PHL)74AS138 =10ns]. This select signal is gated with the /RD signal and the /OE of the 74AHCT374 goes low after a maximum time of t(PHL)74AS32 = 5,8ns. Data is valid after a maximum time of t(a)+t(1)+t(3) = 27ns +10ns +5,8ns = 42,8ns. This is very much

INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	LINK IN	LINKS OUT
/INT0	L46	L44,L8,L39,L40,L35,L43,L45
/INT1	L44	L46,L8,L39,L40,L35,L43,L45
/INT2	L8	L46,L44,L39,L40,L35,L43,L45
/INT3	L39	L46,L44,L8,L40,L35,L43,L45
/INT4	L40	L46,L44,L8,L39,L35,L43,L45
/INT5	L35	L46,L44,L8,L39,L40,L43,L45
/INT6	L43	L46,L44,L8,L39,L40,L35,L45
/INT7	L45	L46,L44,L8,L39,L40,L35,L43

TABLE 5

MULTIBUS ADDRESS DECODING TABLE

/ADR7,/ADR6,/ADR5,/ADR4	LINKS IN
0	L35,L56,L10
1	L39,L56,L10
2	L40,L56,L10
3	L43,L56,L10
4	L46,L56,L10
5	L45,L56,L10
6	L44,L56,L10
7	L8,L56,L10
8	L35,L11,L9
9	L39,L11,L9
A	L40,L11,L9
B	L43,L11,L9
C	L46,L11,L9
D	L45,L11,L9
E	L44,L11,L9
F	L8,L11,L9

TABLE 6

less than the 101,2 ns data setup time required by the processor before /STRB goes high using one wait state. After /STRB goes high the output of the latches enter high impedance state after a maximum time t(DF) +t(2) + t(3) = 33,8ns which is less than the 50ns required by the processor. Therefore bus conflict is avoided.

CHAPTER 9

9.0 KEYPAD INTERFACE

The keypad interface was designed into the system to facilitate an integrator reset. This interface can also be used for other user functions should this be neccessary. Provision has been made for eight seperate function switches that can be incorporated into the operator panel interface.

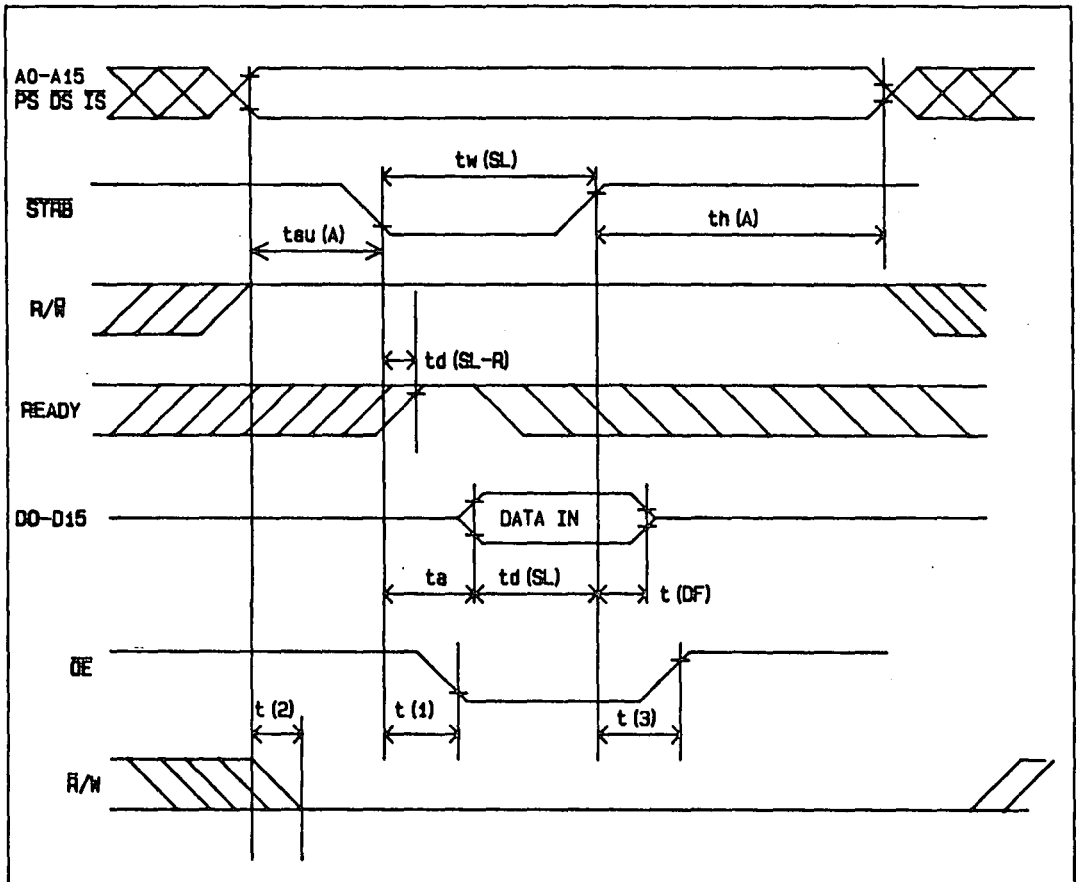
9.1 The Circuit

This comprises a simple tristate buffer. All the input lines are pulled high. A switch would be connected to each of the inputs of the latch. The other end of the switch would be tied to zero volts. A switch closure would pull the corresponding input low. This event would generate an interrupt. A read of this latch would be performed by the microprocessor and the program would be structured to allowing for switch debouncing.

9.2 Timing (Refer to Fiqure 29)

The push button interface is mapped into the I/O space. The read of the latch is performed with one wait state. 13ns after address is valid /STRB goes low. After a maximimum propogation delay of t(1) = 15,8 ns, the /CS select line goes low. This signal gated with /RD. Data at the output of the latch is valid after a

FIGURE 29. READ CYCLE OF 74AHCT373 BY TMS320C25 (ONE WAIT STATE)



SIGNAL DESCRIPTION	SYMBOL USED	VALUE
Address Setup Time	tsu (A)	13ns (min)
Ready Valid after $\overline{\text{STRB}}$ Low	td (SL-R)	105ns (max)
$\overline{\text{STRB}}$ Low Pulse Duration	tw (SL)	100ns (max)
Address Hold Time	th (A)	17ns (min)
Data Setup Time	td (SL)	55, 2ns (min)
Data Disable Time	t (DF)	33, 8ns (max)
Propogation Delay -74AS138		
and 74AS32	t (1), t (3)	15, 8ns (max)
Propogation Delay -74AS04	t (2)	4ns (max)
Access Time of 74AHCT373	t (a)	29ns (max)

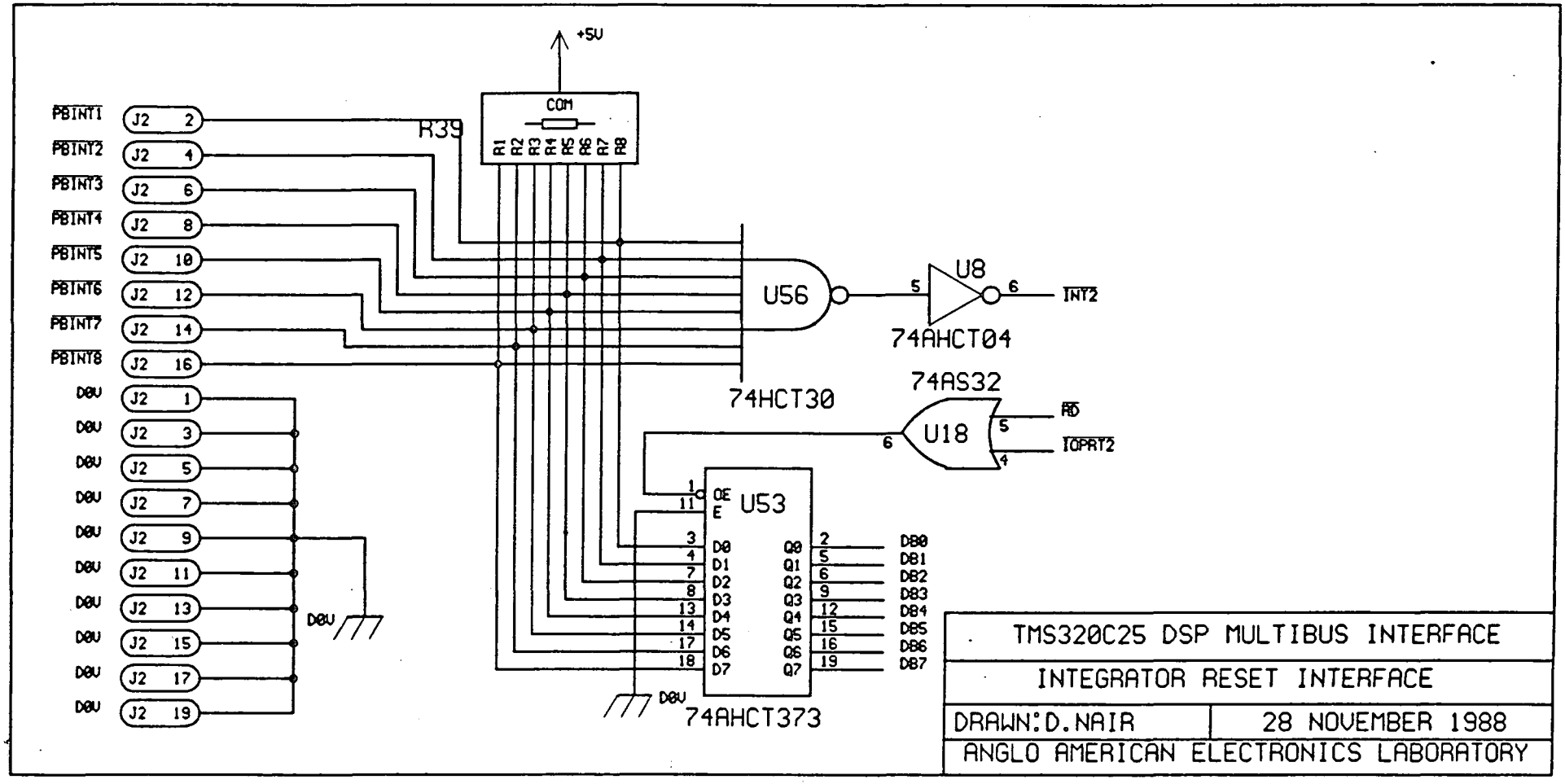

+5V
COM
R39
R1 R2 R3 R4 R5 R6 R7 R8
PBINT1 J2 2
PBINT2 J2 4
PBINT3 J2 6
PBINT4 J2 8
PBINT5 J2 10
PBINT6 J2 12
PBINT7 J2 14
PBINT8 J2 16
D0U J2 1
D0U J2 3
D0U J2 5
D0U J2 7
D0U J2 9
D0U J2 11
D0U J2 13
D0U J2 15
D0U J2 17
D0U J2 19
U56
74HCT30
U8
74AHCT04
INT2
74AS32
U18
RD
IOPRT2
U53
OE
E
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
74AHCT373
TMS320C25 DSP MULTIBUS INTERFACE
INTEGRATOR RESET INTERFACE
DRAWN: D. NAIR
28 NOVEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 30

maximum time of t(a) = 29ns. This is very much less than the 77ns required after /STRB goes low with one wait state. After /STRB goes high the output of the 74AHCT373 buffer is tristate after a maximum time of t(3) + t(DF) =28ns. This is much less than the 50ns required to prevent bus conflict.

CHAPTER 10

10.0 SCHEMATIC CAPTURE AND LAYOUT OF PCB

The printed circuit board was designed using a CAD software package. The advantage of using a CAD package with netlist generation is that on complex digital boards the chances of making an error in the routing of the tracks is almost nil. Advanced design rule checking faclities ensure that design rules are adhered to and a continuity check can be performed on the PCB database.

Because analog and digital circuits are to be routed on the same circuit board, special considerations had to be taken into account in the placement of the various components, and in the routing of digital tracks.

The data acquisition section of the system was grouped together to minimise digital feedthrough from the processor and its peripheral circuits. High speed CMOS circuitry ensured that radiated noise was kept to a minimum.

After placement the average number of pins per square cm was calculated to determine the track density of the circuit board. It was established that the best option was to go to multilayer technology. Circuits using high clock speeds, (40 Mhz in our case) radiate a considerable amount of spurious noise and power and ground planes are necessary to shield sensitive circuit from

this noise. Poor shielding results in circuits toggling randomly, leading to erratic circuit behavior.

The Advanced Schottky family of devices which are used in this design draw large transient currrent during state transitions; if power and ground lines to these devices have a high impedance, large spikes are superimposed on the lines. These spikes often affect other devices down the line. Bypass capacitors can only go so far to alleviate these spikes. Power and ground planes in conjunction with bypass capacitors deliver consistent low impedance power to all devices on the PCB. The way this is done is explained below:

> A ground plane is a conducting surface that is to serve as a return conductor for all current loops in the circuit. All grounded points in the circuit go not to a grounded trace on the PCB but directly to the ground plane. This leaves each current loop in the circuit to complete itself in whatever configuration yields minimum loop area. Thus if a given signal zigzags its way across the PCB, the return path for this signal is free to in the ground plane in such a configuration as to minimise the energy stored in the magnetic field produced by this current loop. Minimal magnetic flux means minimal effective loop area and minimum susceptibility to inductive coupling.

Power and ground planes are generally the innermost layers of the PCB, for two reasons. With PCB material sandwiched between them, the power and ground planes form a bypass capacitor for the supply rails with a low effective series resistance (ESR). The

second reason is that having the planes interior to the signal layers, sensitive signal lines can be isolated from noisy lines by placing them on opposite sides of the planes.

The analog ground on the board is taken out via the connector for the analog signal input. This is in keeping with the single point ground which has its star point at the power supply. This minimises voltage drops along the line by using the star point at the power supply as the reference. Provision is also made for an electromagnetic shield to be placed over the data acquisition section.

10.1 Manufacturing of PCB

A file containing the PCB artwork in the Gerber photoplot format was generated and sent to the manufacturing company. Negatives were generated using a laser photoplotter.

The internal PCB power and ground planes were shorted out through the card remover finger holes because these holes were through hole plated. The through hole plating was drilled out and this sorted out what could have been a very expensive problem.

This completed the manufacture of the first two prototype PCBs.

CHAPTER 11

11.0 DEBUGGING THE HARDWARE

The first components to be inserted into the PCB were the decoupling capacitors, pullup and pulldown resistors. IC sockets were inserted next. Power was applied to the PCB and the power supply was checked at all the relevant pins.

The hybrid oscillator was installed and the clock measured. This functioned as required. Reset circuit and watchdog was then assembled. A NOP instruction was hard wired onto the data bus by using pullup and pulldown resistors. The processor was installed onto the board and powered up. With this arrangement the processor always fetches a NOP as though it is fetching it from memory. The address bus thus behaves as a 16 bit counter, with the address line zero (AO) showing the highest frequency, and A15 the lowest frequency. Program space decoder was installed next and the outputs of the decoder was checked.

The wait state generator components was installed. All remaining decoders and other interface circuitry was installed. The board was now ready to be evaluated on the Extended Development Support System. This offered a very easy solution to check the memory and input/output sections without having to write any software for the system.

11.1 The Memory Problem

The only problem encountered during prototyping was a serious problem with the RAM. The processor failed to read back correct data at specific memory locations. Using the oscilloscope a a timing check on the read and write cycle times was performed. This agreed with calculated values. Slowing down the processor clock and thus increasing the read and write times failed to yield any success. Slower memory like the 6264 worked very well. Further research revealed that the problem lay in the length of the emulator cable and the length of the tracks on the PCB.

At signal rise times of 5 ns, the maximum lenght of an unterminated line should be 2,5 inches long. The length of some the lines were in the order of 16 inches without including the length of the emulator cable. Problems seemed to be caused by the ringing on the address and data lines. Terminating these lines solved the memory problem.

A feedthrough program for the A-D and D-A was written. This program was used to dynamically evaluate the system. A spectrum analyser was used check for sources of error in the system. Due to good design practises there were no noticeable errors due to either digital or any other form of noise.

CHAPTER 12

12.0 ADDRESS MAP OF 320C25 BOARD

DATA SPACE

RAM = SSM7164-35 (0 WAIT STATES)

Address from 0 to 3FFF

PROGRAM SPACE

Option 1: EPROM/RPROM = WS57C49-B (0 WAIT STATES)

Address from 0 to 3FFF

Option 2: EPROM = 27C128 (1 OR 2 WAIT STATES)

Address from 0 to 3FFF

Option 3: EPROM = 27C128 (1 OR 2 WAIT STATES) + 0 WAIT STATE RAM

Address of EPROM from 0 to 3FFF

Address of RAM from 4000 to 7FFF (RAM=SSM7164-35)

I/O SPACE

PORT 0 = INPUT = ANALOG TO DIGITAL CONVERTER

PORT 1 = OUTPUT = ANALOG INPUT MULTIPLEXER CHANNEL SELECTION

PORT 2 = INPUT = PUSH BUTTON INTERFACE

PORT 3 = INPUT = MULTIBUS DATA FROM MASTER

PORT 4 = OUTPUT = MULTIBUS DATA TO MASTER

PORT 5 = OUTPUT = DIGITAL TO ANALOG CONVERTER AND OUTPUT MULTIPLEXER CHANNEL SELECTION

OTHER

BIO = SAMPLE RATE GENERATOR

INT0 = MASTER INTERRUPT TO 320C25 WITH DATA

INT1 = SPARE

INT2 = PUSH BUTTON INTERFACE

XF = WATCHDOG REFRESH PULSES

N.B. FOR OPTIONS LISTED UNDER PROGRAM SPACE CONSULT THE MEMORY LINK TABLE.

CHAPTER 13

13.0 TEST SOFTWARE

```
0001            ****************************************************
0002            *THIS PROGRAM TESTS THE D-A CONVERTER AND ANALOG MUX*
0003            *DATE 4-03-89                                       *
0004            *AUTHOR:D.NAIR                                      *
0005            ****************************************************
0006 0000
0007       0003 PERIOD   EQU 3
0008       0004 INTREG   EQU 4
0009       0064 XN       EQU 100
0010       0000 ADIN     EQU 0
0011       0005 DAOUT    EQU 5
0012       0001 MUX      EQU 1
0013       0065 ONE      EQU 101
0014       0066 OP       EQU 102
0015       0067 DACH     EQU 103
0016       0068 ZERO     EQU 104
0017       0069 ADCH     EQU 105
0018            *PROGRAM STARTS HERE
0019 0000                 AORG 0
0020 0000 FF80 RESET      B    INIT    *RESET VECTOR
     0001 001F
0021 0012                 AORG 18
0022 0012 FA80 WAIT       BIOZ INPUT
     0013 0029
0023 0014 FF80            B    WAIT    * WAIT FOR BIO
     0015 0012
0024 001F                 AORG >1F
0025            ****************************************************
0026            *INITIALISATION ROUTINE                            *
0027            ****************************************************
0028 001F CE01 INIT       DINT          *DISABLE ALL INTERRUPTS
0029 0020 C800            LDPK 0        *SELECT DATA PAGE 0
0030 0021 5588            LARP 0        *POINT TO AR0
0031 0022 CA00            ZAC           *SET ACCUMULATOR = 0
0032 0023 6068            SACL ZERO     *SET ZERO=0
0033 0024 E168            OUT  ZERO,MUX *SET INPUT CHANNEL MUX TO 0
0034 0025 6067            SACL DACH     *SET OUTPUT CHANNEL = 0
0035 0026 E568            OUT  ZERO,DAOUT
0036 0027 FF80            B    WAIT
     0028 0012
0037 0029
0038 0029
0039 0029 E169 INPUT      OUT  ADCH,MUX *SET INPUT MUX
0040 002A 8064            IN   XN,ADIN  *READ A-D
0041 002B D001            LALK >FFF0    *MASK LOWER 4 BITS
     002C FFF0
0042 002D 4E64            AND  XN       *SET D-A MUX CHANNEL
0043 002E 6064            SACL XN
0044 002F 0067            ADD  DACH
0045 0030 6066            SACL OP
0046 0031 E566            OUT  OP,DAOUT *WRITE TO D-A
0047 0032 D001            LALK 1
     0033 0001
0048 0034 0067            ADD  DACH
0049 0035 6067            SACL DACH
0050 0036
0051 0036 D001            LALK >7
```



```
     0037 0007
```

```
0052 0038 4E67              AND  DACH    *PREVENT OVERFLOW OF
0053 0039 6067              SACL DACH    *CHANNEL NO. TO DATA BITS
0054 003A D001              LALK 1
     003B 0001
0055 003C 0067              ADD  DACH    *INCREMENT CHANNEL NO.
0056 003D 6069              SACL ADCH
0057 003E
0058 003E FF80                       B    WAIT
     003F 0012
0059 0040
0060                        END
NO ERRORS, NO WARNINGS
```

CHAPTER 14

14.0 CONCLUSION

The hardware development of the TMS320C25 was successfully completed. Plate 3 shows the fully populated DSP board. Integration programs were developed for both the contact and area signals. Software development is currently in progress. Although the hardware designed does meet the requirements for the instrument; the most serious drawback is that it is based on the Multibus system. While the board can find numerous applications in other areas of DSP, it is by no means suitable for a portable instrument. For this reason development work is under way to implement a similar system on a much smaller printed circuit board.

With the hardware developed, the Anglo American Electronics Laboratory will surely meet any future requirements that may be demanded of a digital signal processing system.

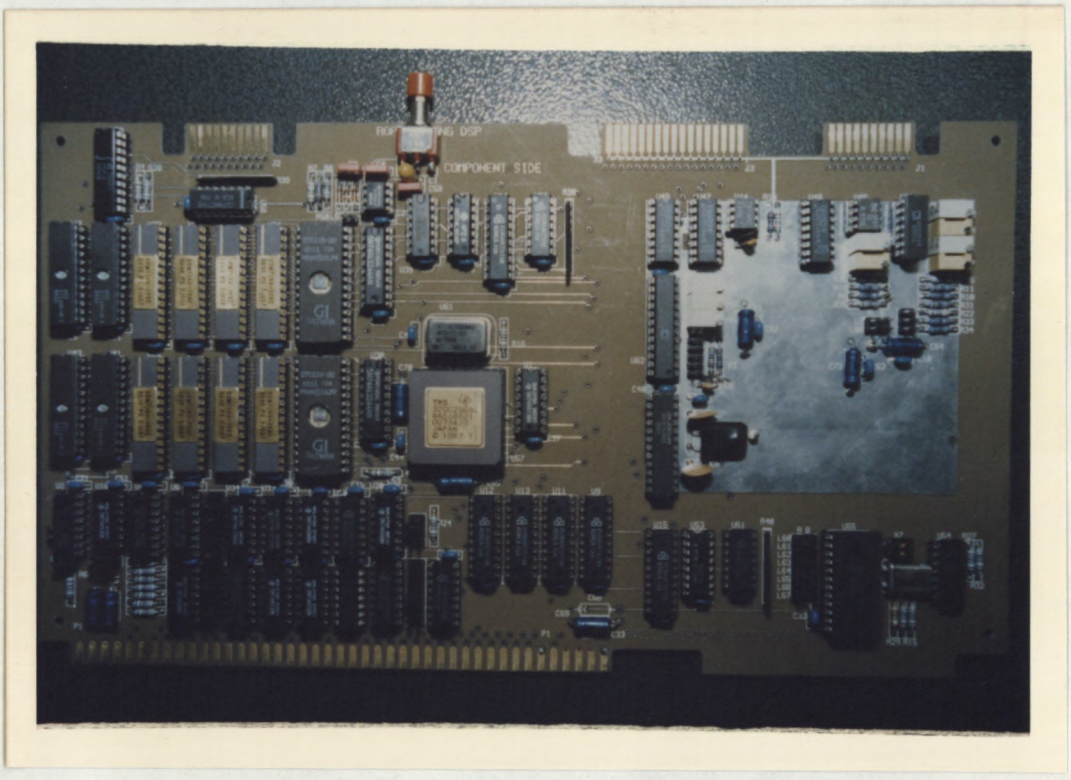


PLATE 3

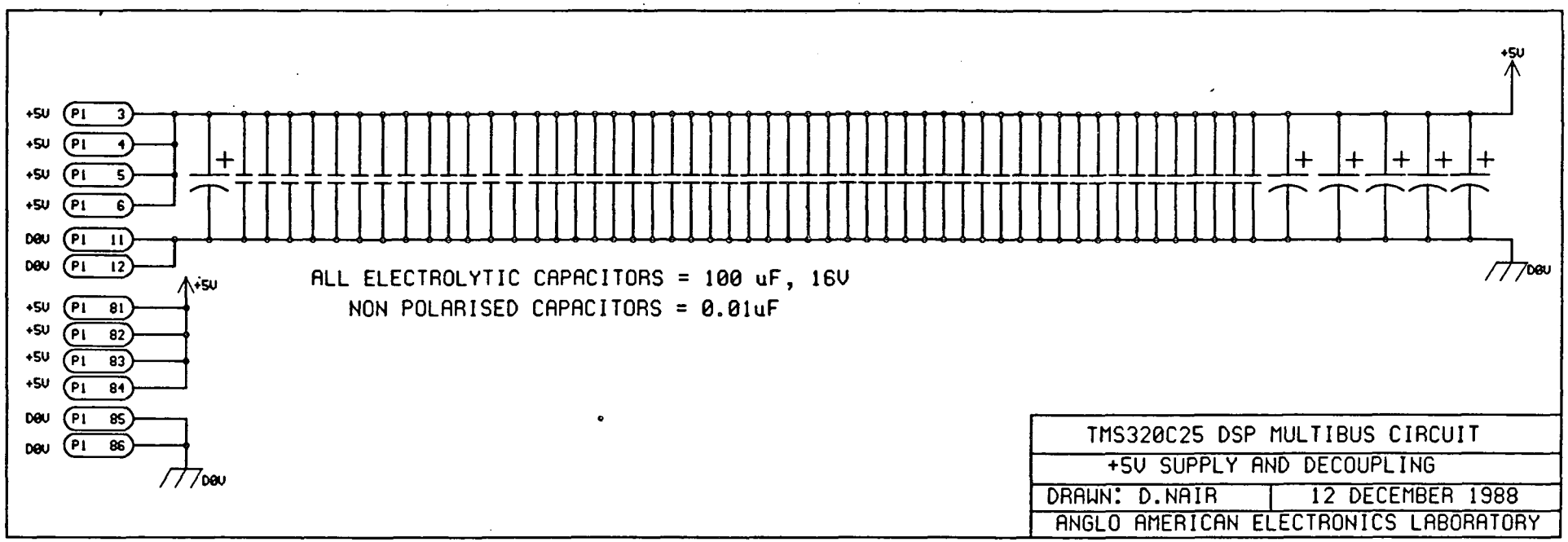

+5V
P1 3
+5V
P1 4
+5V
P1 5
+5V
P1 6
D0V
P1 11
D0V
P1 12
+5V
P1 81
+5V
P1 82
+5V
P1 83
+5V
P1 84
D0V
P1 85
D0V
P1 86
D0V
+5V
D0V
ALL ELECTROLYTIC CAPACITORS = 100 uF, 16V
NON POLARISED CAPACITORS = 0.01uF
TMS320C25 DSP MULTIBUS CIRCUIT
+5V SUPPLY AND DECOUPLING
DRAWN: D.NAIR
12 DECEMBER 1988
ANGLO AMERICAN ELECTRONICS LABORATORY

FIGURE 31

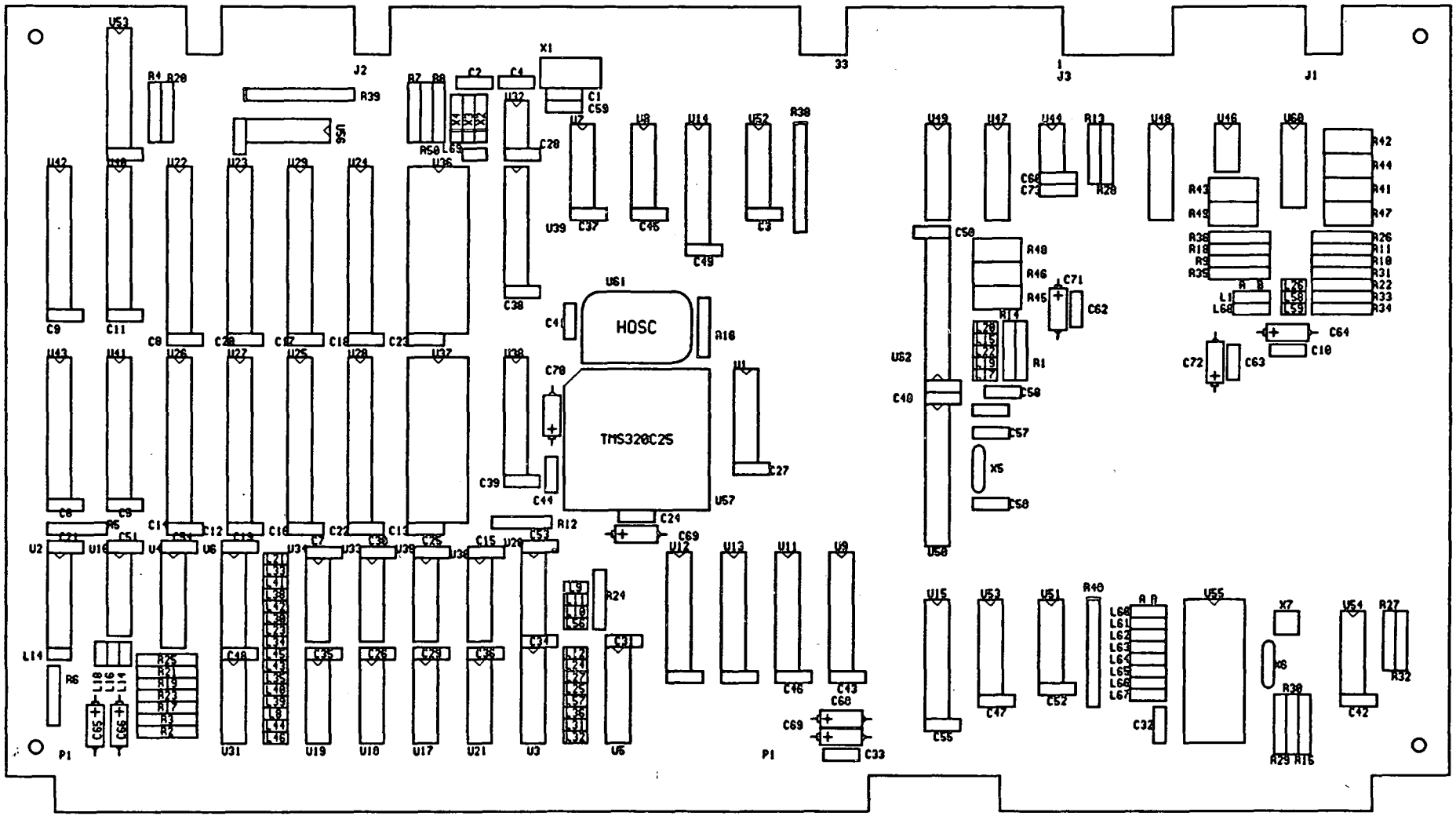


FIGURE 32

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