Transient Fault Analysis of a VSC-Based Multi-Terminal HVDC Scheme.

By

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A thesis submitted in fulfilment of the requirements for the degree of

MASTER OF ENGINEERING IN ELECTRICAL ENGINEERING

DEPARTMENT OF ELECTRICAL ENGINEERING

DURBAN UNIVERSITY of TECHNOLOGY

September 2020

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Durban, 16 September 2020

I humbly dedicate this research project to God almighty, who is my source of wisdom, knowledge and understanding, for his faithful help to complete this thesis.

ACKNOWLEDGEMENT

I would like to thank my main supervisor Professor Innocent E. Davidson, for his consistent support and guidance on the successful completion of this thesis and the numerous valuable inputs. The completion of this research project would not have been possible without his professional and career-building advice. I am extremely grateful for our friendly chats at the end of our research meetings. I would also like to express my thanks to my co-supervisor, Dr. Grain P. Adam,my research team especially Elutunji Buraimoh, my siblings Malibongwe, Zamathuli and Malusi, and my parents Mr. and Mrs. Malanda for their encouragement and endless support.

I wish to acknowledge South Africa Space Science for financial and the opportunity given to me to undergo a Master's degree program.

And last but not least, I am very grateful to my partner Okikiade "Fame" A. Layioye, without his incessant support, I would never have been able to complete this thesis. Fame continuously provided encouragement and was always willing and enthusiastic to assist in any way he could throughout the research project.

ABSTRACT

A multiterminal HVDC system includes the connection of different HVDC terminals to a common grid. Most of the MTDC networks are realized in voltage source converter (VSC) high voltage direct current (HVDC). Over long distances, HVDC transmission is preferred to high voltage direct current (HVAC). Furthermore, HVDC is subjected to minimal harmonics oscillation problems due to the absence of frequency. HVDC enables the interconnection of systems at different frequencies, and the system becomes free of angular stability problems. VSCs employ insulated gate bipolar transistors (IGBTs) switches, and High-frequency pulse width modulation is used to operate the IGBTs in order to achieve high-speed control of active and reactive power. The growth of MTDC networks may require a new type of VSCs topology, which is resilient and efficient to dc and ac network fault. This research investigation focuses on the transient dc-side fault analysis in a two-level Monopolar VSC-Based Multi-Terminal HVDC Scheme consisting of four asynchronous terminals sharing a rated 400kV DC-grid was carried out in PSCAD software. During dc-side fault analysis, a pole-to-ground fault was taken into consideration as it's more likely to occur, although it is less severe compared to pole-to-pole. The converters are interconnected through 100 km dc cables placed 0.5 gm apart and at a depth of 1.5 m underground. It was observed that during the steady-state analysis, the dc voltage in the grid was maintained at the rated value 400 kV, the currents measured at the converters bus was 0.5 kA, and the current flowing through the cables was 0.25 kA. Under the fault condition, the dc voltage drop needs to be maintained to a closed range to avoid the grid to collapse. The voltage droop technique was incorporated in the dc voltage controller to keep the dc voltage at the narrow range. Depending on the value and nature of ground fault resistance, the fault current magnitude varies, and distance variation along the cable has a significant contribution in the fault current. It is observed that fault close to the converter (5 km's measured 9 kA) results in high fault currents compared to fault away from the converter (50 km's measured 7.8 kA). The protection design of the VSC needs to be able to detect whether its ground fault or short circuit since the location of the fault needs to be identified and repaired. Another observation made

when the fault is inserted 50 kms away from the converter, meaning the fault is at the center of the two converters, the outcome results in high currents in both converters. The isolation of the fault should be fast and selective as the critical time is very short. The dc circuit breakers are mostly recommended to be used as primary protection; however, different protection techniques need to be incorporated with dc circuit breaker in order to quickly identify, select and reliable isolate the faulted line. Moreover, the protection should be able to isolate the line before the fault reaches the maximum fault current to avoid the damage in the converter components.

DECLARATION 2-PUBLICATIONS

The following publications were derived from this research investigation.

[1] S. C. Malanda, I. E. Davidson, and G. P. Adam, "Comparison of DC voltage Control Strategies for Multi-terminal HVDC Network during AC Faults," in 2020 International SAUPEC/RobMech/PRASA Conference, 2020: IEEE, pp. 1-6.

[2] S. C. Malanda, I. E. Davidson, E. Singh, and E. Buraimoh, "Analysis of Soil Resistivity and its Impact on Grounding Systems Design," in 2018 IEEE PES/IAS Power Africa, 2018: IEEE, pp. 324-329.

Manuscript submitted to the International Journal of Engineering Research in Africa (JERA). [Under Review]

[3] S. C. Malanda, I. E. Davidson, M. N. Chamane, and M. N. Gitau, "A Comparison of the Transient Characteristics of a Two-Level VSC and Half-Bridge MMC Protection Scheme."

Manuscript submitted to Energies MDPI [Under Review]

[4] I. E. Davidson, M. N. Gitau, M. N. Chamane, and S. C. Malanda "Analysis of DC Fault Protection Scheme for a Multi-Terminal Direct-Current VSC-HVDC Based System."

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LIST OF ABBREVIATIONS

A	Amps
AC	Alternating Current
ASMD	Adjustable Speed Motor Drive
CHB	Cascaded Half Bridge
CB	Circuit breaker
CCC	Capacitor Commutated Converter
DC	Direct Current
EMTP	Electromagnetic Transients Program
FB	Full-Bridge
FC	Flying Capacitor
FACTS	Flexible Alternating Current Transmission Systems
H	Inductor
HVDC	High Voltage Direct Current
HB	Half-Bridge
HVAC	High Voltage Alternating Current
I	Current
Imax	Maximum Current
Irated	Rated Current
Iqmax	Maximum Reactive Power Current
ICC	Inner Current Controller
IGBT	Insulated Gate Bipolar Transistors
LCC	Line Commutated converter
MW	Megga Watts
MMC	Modular Multilevel Converter
MTDC	Multi-Terminal Direct Current
NPC	Neutral-Point-Clamped
NERSA	National Energy Regulator of South Africa
OHL	Over-Head Lines
P	Power

PCC	Point of Common Coupling
PLL	Phase Lock Loop
PI	Proportional Integrator
PWM	Pulse Width Modulation
PU	Per Unit
Q	Reactive Power
RE	Renewable Energy
R	Resistance
RoW	Right of Way
SAPP	Southern African Power Pool
SVM	Space Vector Modulation
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
VSC	Voltage Source Converter
V_c	Capacitor Voltage
V_s	Voltage Source
XLPE	Cross-Linked Polyethylene

CHAPTER 1: INTRODUCTION

1.1 Background Study

South African state-owned electric utility named Eskom is still heavily dependent on coal as its primary source of electricity due to large coal reserves[1] [2]. Economic development in South Africa is mainly driven by reliable electricity supply [3]. During the 1990s, South Africa's power generation was highly stable and reliable with a significant surplus capacity [4], unlike many sub-Saharan and sub-Equatorial African countries with limited electricity infrastructure [5]. Presently, high power demand caused by a combination of factors such as high population growth, load growth, rapid economic expansion, and nearby countries inadequate electrical power supply system led the country and neighboring countries to instabilities, which resulted in periodic-load shedding. The availability of electricity is vital in every sector; therefore, the power grid should be reliable [6]. A standard and reliable power grid should have the following features or qualities: the grid voltage generated should be within limits, must be able to withstand the loss of a generator, transmission line must be able to retain stability during faults, and must not be overloaded, and lastly, the generating capacity must be greater than the demand [7]. The approval of constructing Kusile and Medupi coal power stations in 2007 by the National Energy Regulator of South Africa (NERSA) was driven by the annual production of coal rise by a factor of 119% to meet the ever-increasing consumer demand. Coal power plants contribute about 82.6% out of 44 134 MW nominal capacity, but most of these plants lack efficiency since they are over 20 years old, and they will soon reach their life span limit [4]. The construction of new power plants will increase the electricity tariffs due to lack of capital, and on the other hand, the government projection by 2030 is to have renewable energy (RE) sources representing 20% of the total installed capacity [8]. Currently, high voltage direct current (HVDC) technology and dc grids are linked to green energy to incorporate large-scale renewable energy plants.

South Africa is one of the countries which participate under Southern African Power Pool (SAPP) where power systems are interconnected to other

countries. Such interconnection influence each countries operation [9]. The interconnection of South Africa includes Mozambique (Cahora Bassa hydropower) through HVDC transmission (2 x 533 kV DC lines, 1700 MW), Swaziland at 400 kV, Namibia at 400kV and 220 kV, Lesotho at 132 kV and Botswana at 400 kV [1]. The continent of Africa is divided into five regions shown in Figure 1.1, occupying about 20% of the world which covers 30 million square kilometers with high potentials of the primary sources of energy such as coal in Southern region, oil and gas North region, and hydro resources which are available in the central region [5].

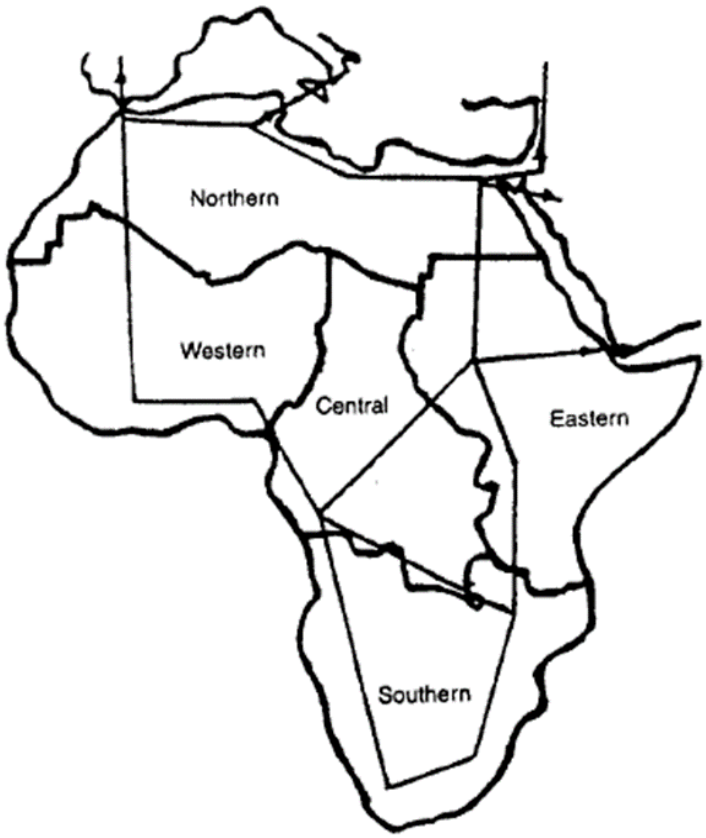
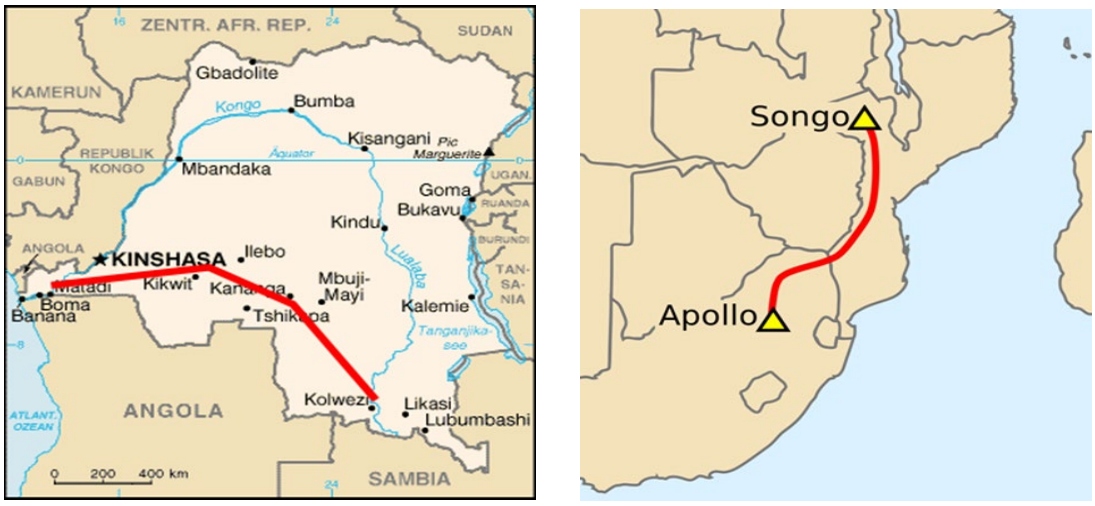


Figure 1. 1 African regional power pools [5].

Grand Inga River, located at the heart of Africa, in particular, the Democratic Republic Congo, is the world's largest untapped hydropower potential since it crosses the equator twice and has a total length of 4.370 km. The hydro potential is estimated to deliver about 100000 MW capacity of clean, sustainable, and green renewable energy when considering the upper and lower stream. The possible development of the hydro-electric project, wind

power, and solar-PV can sufficiently electrify the whole of Africa and trade power to European countries. The proposal of integrating the Africa power grid into a smart integrated Africa electric power super grid through the use of HVDC technology will enable the large penetration of renewable power without compromising the power system and voltage stability, active and reactive power flow and power quality [10].

The generated power from hydropower station and wind farms are usually found far from the load centers and has to be transmitted over long distances using the most reliable and efficient bulk power transmission system [2] for example, and the Inga–Shaba Extra HVDC Intertie shown in Figure 1.2(a) is 1,700 kilometers (1,100 mi)-long high-voltage direct current overhead electric power transmission line [11] [12]. Over long distances, HVDC transmission is preferred to high voltage alternating current (HVAC). Furthermore, HVDC is subjected to minimal harmonics oscillation problems due to the absence of frequency. HVDC enables the interconnection of systems at different frequencies, and the system becomes free of angular stability problems [10]. HVDC transmission systems are available in point-to-point, back-to-back and multiterminal direct current (MTDC) grids. Over long distances, the point-to-point system is used to transmit a large amount of power from generating stations to the load centers. A back-to-back system is different from a point-to-point system, both rectifier and inverter of the back-to-back are located at the same building, and they are generally used to connect ac grids operating at different frequencies or areas that may be asynchronous. These are the most used HVDC configurations in the world. As presented in Figure 1.3, the HVDC system installed capacity is growing exponentially [13]. Line commutated converter (LCC) or capacitor commutated converter (CCC) and voltage source converter (VSC) are the two types of HVDC transmission systems used [14] for medium voltage, HVAC and HVDC [15].



(a) Inga–Shaba EHVDC (b) Cahora Bassa-Apollo HVDC

Figure 1. 2: (a) HVDC power transmission system between Inga–Shaba EHVDC in DRC and (b) the Cahora Bassa Hydroelectric Generation Station at the Cahora Bassa Dam in Mozambique, and Apollo in Johannesburg, South Africa

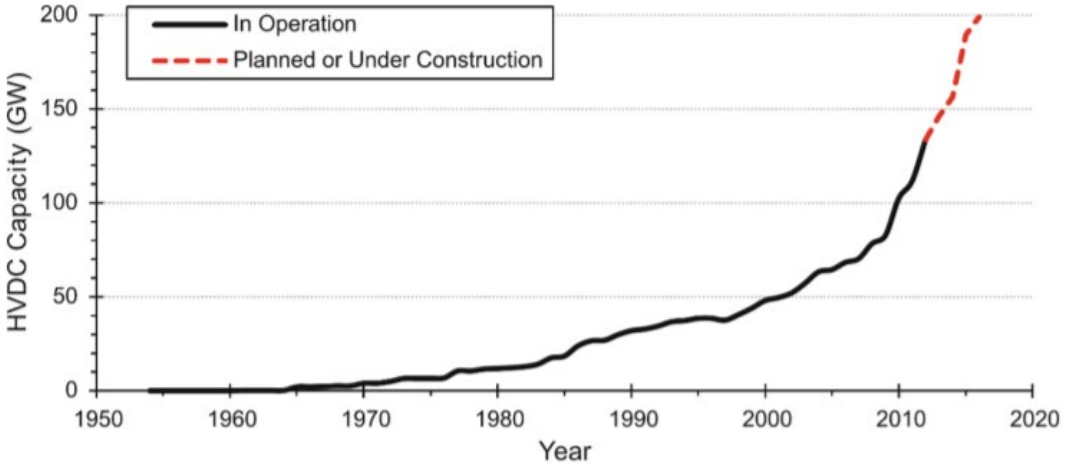


Figure 1. 3: Installed HVDC system worldwide [13].

Cahora Bassa Hydroelectric Generation Station at the Cahora Bassa Dam in Mozambique import energy to Johannesburg (Apollo) as shown in Figure 1.2(b) to supplement South Africa grid using LCC-based HVDC power transmission system with thyristors as their switching devices [12], which is one of the existing HVDC point-to-point connection in the world. The first HVDC link was successfully commissioned in 1954 between Gotland and Swedish mainland [16]. However, several constraints are associated with the LCC thyristor-based, such as the inability to fully control active and reactive

power independently, thyristor switching characteristics, harmonic currents, and large footprint [17]. Moreover, the Integration of renewable energy sources, which usually consist of weak grids due to the short circuit ratio, is limited in LCC technology. The absence of power-direction control hinders the application of large scale MTDC HVDC systems where all converter stations share the same grid [18].

The development of power electronics led to new HVDC transmission generation based on VSC, which employ insulated gate bipolar transistors (IGBTs) switches. High-frequency pulse width modulation (PWM) is used to operate the IGBTs in order to achieve high-speed control of active and reactive power. VSC technology provides several potential features when compared to conventional HVDC [19]. Several advantages offered by VSC-HVDC technology includes black start capability [20], lower losses, grid access for weak network, independent control for active and reactive power, the supply of passive networks, interconnect asynchronous networks and multiterminal and low environmental impact. The power reversal capability in VSCs brought back significant interest in the establishment of the MTDC network like super grids. The growth of MTDC networks may require a new type of VSCs topology, which is resilient and efficient to dc and ac network fault. Half-bridge (HB) and full-bridge (FB) modular multilevel converter (MMC) are already existing converter topology with the potential to meet some of these requirements, and several hybrid converters are proposed [21]. The most common topologies used for the MTDC grids system are based on two-level VSC topology and HB MMC [22]. Major MTDC projects are already in operation, and some are in advance design stages worldwide [19] [23]. On December 25th, 2013, the first world MMC-MTDC was officially commissioned successfully in China. The Nan'ao VSC-MTDC system has a design rating of 160kV dc voltage, and the converter employs symmetric monopole configuration. However, VSC-HVDC converters are prone to dc line fault [23] [24] [25], high fault current has a possibility of damaging the systems equipment such as insulation of the cables, IGBT switches and destroy the diodes of the converter terminal [22].

The interconnection of the dc side transmission system of more than two converter stations is classified as an MTDC network [26], which is further categorized by its configuration according to the HVDC technology type implemented at the converter station. MTDC networks can be simply built by tapping from the existing point-to-point terminal, but this will introduce complexities of control and protection. Furthermore, telecommunication may be required between the stations [27]. For multi-terminal scheme to be developed successfully, detailed analysis of four key aspects is required namely: fault behaviour, power flow control, system integration and dynamic behaviour [28] [29]. Unlike point-to-point HVDC transmission control where only one terminal is assigned to control dc network voltage, in MTDC network it becomes difficult to apply the same strategy due to dc side interconnection. To ensure power sharing balance in MTDC, multiple converters should have access to dc voltage control. The concept of Africa super-grid can be realized for multi-renewable sources connection which are readily available in the continent and integration to different ac grids around the continent. Therefore, the grid will results into meshed grid topology. VSC-MTDC network has a great flexibility for large-scale renewable energy integration and transmission network, however MTDC protection is still a major challenge in the event of a fault at the dc-grid. The presence of low impedance in the dc network results in high rate of current rise during dc side fault [30].

The VSC-HVDC converter topology depends on the semiconductor switches arrangements and can be classified either as a two-level or multilevel. Two-level VSC has a simple configuration, robust and reliable, but the topology suffers from high dv/dt, high conversion losses and requires a special transformer with high insulation requirements. On the other hand, multilevel converters have low dv/dt, low conversion losses, use smaller ac filter compared to two-level, and uses a transformer with a relatively low insulation requirement [14]. Even with attractive features of multilevel converters, most of the converters in operation are based on VSC two-level topology. In Africa, the first VSC-based transmission system was commissioned in 2010, the Caprivi Link interconnector between Namibia and Zambia showed in Figure 1.4 [11]. The overhead line is 950 km's long and operated at -350 kV dc [31].

The Caprivi Link can be extended to an MTDC transmission and form Africa super-grid, it can be further connected into the Congo River in order to electrify the whole continent.

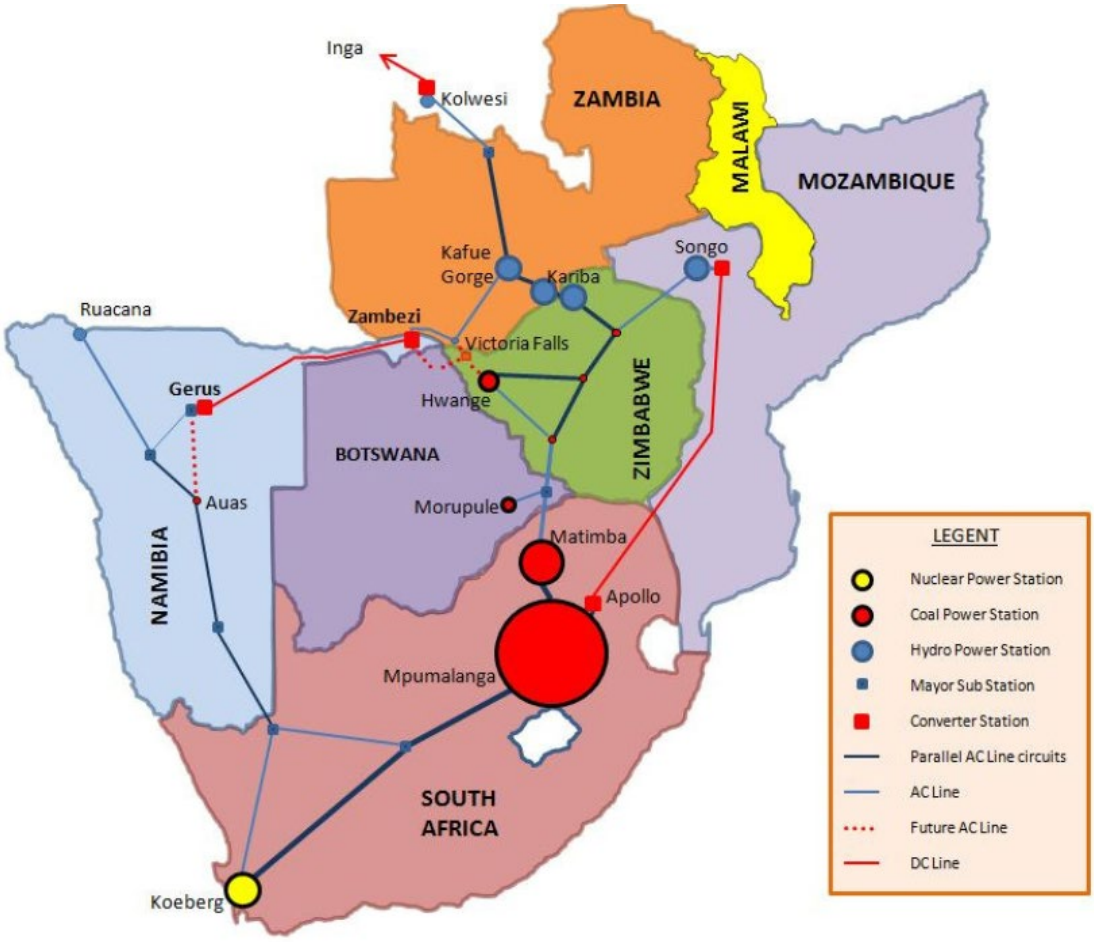


Figure 1. 4: VSC-HVDC Caprivi Link interconnector between Namibia and Zambia [31]

Most upcoming MTDC HVDC transmission systems are expected to employ multilevel topology known as MMC. The development of MMC introduced different characteristics compared to conventional two-level and three-level, such as less filter size, scalability, and high-quality output voltages. Some researchers proposed that the MMC topology has intrinsic dc fault blocking capabilities. Several MMC topologies with fault-current blocking capability are based on full-bridge sub-modules MMC and are discussed in detail in [32], while other new topologies are hybrid based on half and full-bridge, series-connected double modules, clamp-double submodules, alternative-arm converter and hybrid arm bipolar [33]. However, a detailed understanding of

the two-level system can offer useful guidance for analyzing other systems using different converter topology [34]. Thus, a thorough analysis of dc fault in MTDC is essential in order to get a better understanding of its behavior during dc-side faults.

1.2 Problem Statement

Underdeveloped power network and inadequate generation systems in the African continent still leave millions of people without electricity in Africa, despite the establishment of regional power pools and large energy endowment. Almost two-thirds of Africans do not have access to electricity. Power deficiency is believed to delay economic growth in Africa economies. Increasing population and urbanization are taken as some of the key factors driving up electricity demand. Consequently, there is a crucial need to increase and improve the capacity of the power sector in Africa. Available renewable energy (RE) sources in Africa are a preferred solution to meet the energy demand for sustainable development. Renewable sources introduce energy mix, which highly influences the future grids in a number of ways. However, renewable sources are mostly located far away from the load centers and require to be transmitted over long distances to be integrated into the main grid.

HVDC transmission, which is the preferred bulk power transmission system, is the preferred technique that can be used to overcome this problem over the HVAC transmission system. HVDC transmission systems present minimal transmission losses, low cost over long distances, and are environmentally friendly. Presently, VSC-based HVDC technology is used for HVDC projects, since LCC-based HVDC is not suitable for RE sources integration into the grid. However, VSC-HVDC systems are vulnerable to dc-side faults. During the occurrence of the dc-side fault, IGBTs could be blocked for self-protection, and anti-parallel diodes act as a bridge rectifier and feed the fault. Some of the key challenges for the MTDC system are a thorough understanding of the system behavior when subjected to various faults such as dc-side fault conditions, as this will ensure that the most efficient protection protocols can be developed.

1.3 Objectives of the Study

This research investigation aims to analyze transient dc-side fault in a two-level Monopolar VSC-Based Multi-Terminal HVDC Scheme consisting of Four asynchronous terminals sharing a rated 400kV DC-grid. The research objectives of the study are given as follows:

(i.) Develop a VSC-based HVDC-MTDC test model using PSCAD software package comprising of:
- Four meshed monopolar, two-level VSC-HVDC converters interconnected into a dc-grid.
- All converters will be connected through the use of dc-cables at rated dc voltage.

(ii.) To investigate transient fault and their influencing factors in multi-terminal HVDC networks.

(iii.) Analyze the influence of the components main parameters on the transient fault current development during pole-to-ground faults, as well as the interaction between these components by means of simulations.

(iv.) Identify and quantify the major fault current influencing factors, i.e. transmission technology, network topology, and network grounding schemes.

1.4 Research Questions

The research investigation is formulated by the following questions:

- To what extent will the transient fault current affect the multi-terminal network, and how will the fault impact the power-sharing of this network?
- At what stage will the VSC main components be influenced by the development of transient's fault current through the pole-to-ground fault?
- How would the fault's location affect the network?

1.5 Significance of the Study

This research will provide a detailed design of a Multi-terminal VSC-based HVDC transmission network and a better understanding of system behaviour under dc-side fault condition that will be of significant use to the Africa super-grid and South Africa power projects proposals in terms of integrating renewable sources into the grid.

1.6 Research Contribution

To date, there are several point-to-point HVDC systems in operation worldwide, but only a few multi-terminal HVDC (MTDC) networks have been implemented. Two-level VSC topology will be implemented in a multi-terminal network using dc cables for transmission in this research. The control approach that is to be used in this study has only been used in a point-to-point network.

1.7 Limitations and Delimitations

This research is limited to high voltages that are being proposed and used by Eskom in their transmission lines. This multi-terminal network can use different sources like renewable energy (wind farm and solar) in different places, but in this work, only fixed ac sources will be used. This research is limited to transient fault analysis in a multi-terminal network using software simulation tools only and using available software: Electromagnetic Transients Program (EMTP) DC /PSCAD

1.8 Thesis Arrangement

The arrangement of this thesis includes five chapters with chapter 1 presenting introduction, background, problem statement, and motivation. Chapter 2 introduces a theoretical knowledge for a better understanding of the voltage source converters, high voltage direct current technology and their limitations, converter topologies, control structure, and basic components. Chapter 3 focuses on the ac and dc-side mathematical modelling of a two-level converter. Chapter 4 provides a description of the developed model in PSCAD. Finally, simulation and results are provided in chapter 5, and the thesis concludes with a brief summary of the model results.

CHAPTER 2: LITERATURE REVIEW

The main objectives of this chapter are to provide an overview of HVDC technology and briefly discuss why is it preferred than a conventional HVAC, Transmission configurations of HVDC and HVDC topologies known as Line Commutated Converter and Voltage Source Converter. Furthermore, the chapter discusses the operating principles of a VSC-based HVDC transmission system and components of the system. Moreover, the chapter covers the grounding configuration, the technique used for VSC control.

2.1 Overview of HVDC Transmission Systems

2.1.1 HVDC Technology

The preferred option for interconnection is High voltage (HV) because it leads to low line losses compared to medium voltage. For interconnection, HVDC and HVAC type can be used depending on which one of them is found to be technical and economical [35]. HVDC transmission offers several operational advantages such as transmitting bulk electrical power efficiently over long distances, minimal problems of harmonics, and mostly it can interconnect unsynchronized AC network at different frequencies, unlike HVAC transmission systems. The existence of inductance and capacitance in the AC transmission leads to reactive power loss as well as the carrying capacity is the issue to the AC lines.

Moreover, power flow control is the most important technical aspect which should be addressed when choosing the type of connection. The power flow control in HVDC can be achieved by changing voltage polarity or by changing the current direction, but HVAC power control requires supporting equipment such as unified power flow control and phase shift transformer. In comparison, HVDC is found to be more economical when looking into the total cost of building the system. The footprint of HVDC is less than the HVAC system with the same rating. Figure 2.1 shows the comparison between the HVAC and HVDC systems, including building station cost, cost of the line, and losses at different distances.

The breakthrough of HVDC technology was recorded in Gotland 1954 using undersea cables interconnection, and for long-distance transmission schemes, mercury-arc valves were utilized. In 1972, thyristors valves were introduced, replacing mercury-arc valves in the first back-to-back asynchronous interconnection between Quebec and New Brunswick[16] [35].

2.1.2 HVDC Technical Evaluation

Problems associated with ac transmission technology can be solve using HVDC technology [35]:

- **Voltage control:** Line charging and voltage drop complicate the control of voltage in the line. Normally dc line doesn't require reactive power equipment, even though the converter requires reactive power associated with power transmitted. On the other hand, ac transmission maintains its constant voltage by using reactive power control as the line loading increased. The length of the line is also a factor in reactive power requirements. Furthermore, the distance for cable transmission is limited around 50km's due to steady-state charging currents [35].
- **Line compensation:** External equipment such as series capacitors, shunt inductors, Static Var Compensators, and STATCOM are required in ac transmission in order to increase the power transfer and voltage control. There is no need for compensation in dc lines.
- **Stability Limits:** In an ac transmission, power transfer depends on the angle difference between the voltage angles at the two-line ends. Consequently, maximum power transfer is limited by transient stability and steady-state. Transmission distance in an ac system affects the power carrying capability of the line. In dc lines, the distance of transmission does not affect the power carrying ability.
- **Ground Impedance:** In dc links, one conductor negative/positive with ground return can be used.

HVDC transmission is advantageous compared with conventional AC transmission due to the following reasons [36] [37] [38] [39]:

- HVDC cable power losses are lower, and cable cross-section is low.

- There is no need for reactive power (Var) compensation along the line.
- For the two AC areas, there is no synchronization required.
- Converters can provide the necessary support to the grid-like damping oscillation, voltage regulation, and synthetic inertia (only for VSC_HVDC).
- It is cheaper for distances more than 500 km for Over Head Lines (OHL) or 40 km for underground cables.
- Improves fault ride through capability of the system.
- Large-scale power transfer

HVDC technology has its own drawbacks, namely [40] [35]:

- Generation of harmonics in converters and require a filter.
- Cost of converters
- MTDC networks are challenging to implement
- The controls of the converter system are complex
- Unlike the ac system, where voltage can be altered with the use of transformers, the HVDC system is unable to alter voltage levels.

The total cost of HVDC and HVAC transmission is graphically represented in Figure 2.1, and it is based on economic and technical factors such as costs, transmission distance.

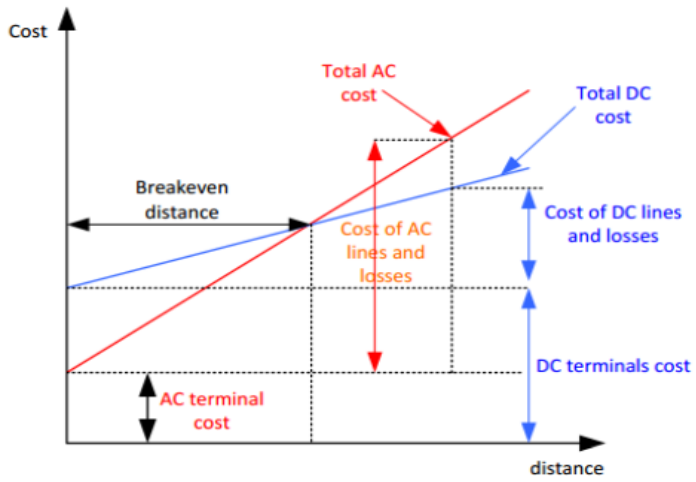


Figure 2. 1: AC and DC system cost breakdown [41].

Two possible ways to connect HVDC transmission can be submarine/underground cable or overhead lines. Generally, HVDC topologies depend on the type of power device used for converters and can be categorized as a line-commutated converter and forced-commutated converter.

Line-commutated converter: Semi-controlled power devices like thyristor are used to build this type of the converter, and its commutation is dictated by the polarity change of the grid voltage. Normally, it is applied in the full-bridge topology for LCC-HVDC.

Forced-commutated converter: Fully controlled power devices that are used for this converter are called IGBTs and IGCTs. These devices can control both turn-off and turn-on commutation, and it is typically used in full-bridge topology in VSC-HVDC. VSC topology uses Pulse Width Modulation for switching.

2.1.3 HVDC Transmission Configuration

Usually, HVDC systems are configured as bipolar or monopolar. The application of bipolar configuration is much expensive when compared to the monopole because it uses two ground-isolated lines, and for each terminal, at least two converters should be used. However, this configuration has advantages in the area of system protection and redundancy due to the double power injection. In bipolar topology, transformers which link ac grid and converters are of different groups or transformer with two windings [42]. Generally, for harmonics reduction configuration for both transformers won't be the same. Normally one transformer uses grounded-star to delta transformer connection, whereas the other uses grounded-star-star. The increased flexibility offered by the bipolar configuration makes it be the favorite in the future HVDC grid development. With support from the bipolar, the DC grid can have several possible configurations, namely: bipole with metallic return and bipole with the ground return [24] [29] .

(a) Bi-pole with metallic return illustrated in Figure 2.2: Unlike bipole with ground return, metallic return requires an extra-low voltage insulated neutral conductor.

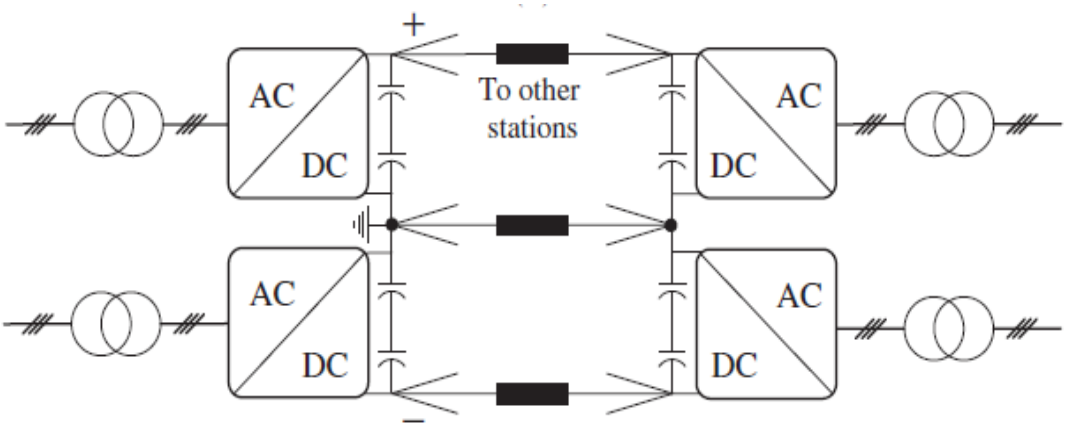


Figure 2. 2: Bi-pole grid with metallic return.

(b) Bi-pole with ground return shown in Figure 2.3: Environmental impact is a major concern due to ground currents where both poles are not balanced in this configuration.

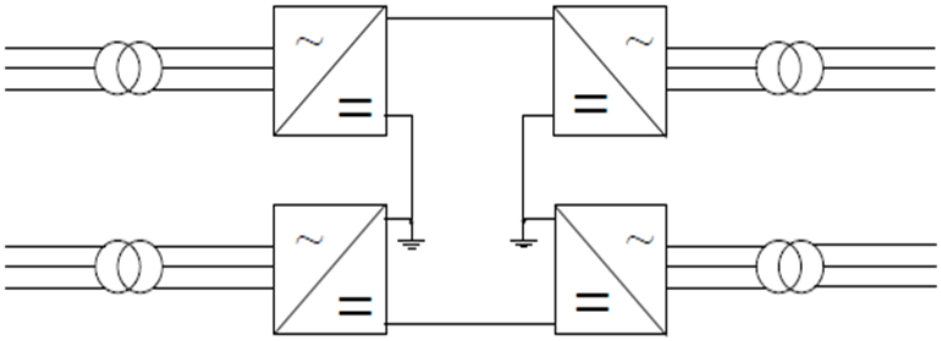


Figure 2. 3: Bi-pole grid with ground return.

Monopolar topology employs only one pole at the network terminal. The negative polarity is mostly used to reduce corona effects. The classification of monopolar is as follows [42]:

(a) Asymmetrical Monopole with ground return: The use of a single conductor, as presented in Figure 2.4, which is fully insulated, is an advantage in this topology from a cost perspective. Thus, it can be expanded into a bipolar topology if necessary. However, it raises environmental issues in terms of the installation of electrodes and continuous ground currents [37].

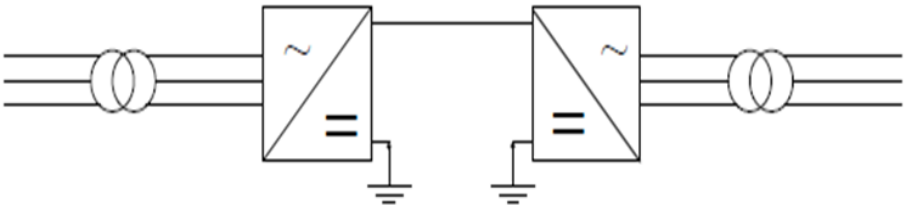


Figure 2. 4: Asymmetrical Monopole grid with ground return.

(b) Asymmetrical Monopole with metallic return: The metal conductor is used as a return, as shown in Figure 2.5, and does not require high-voltage insulation.

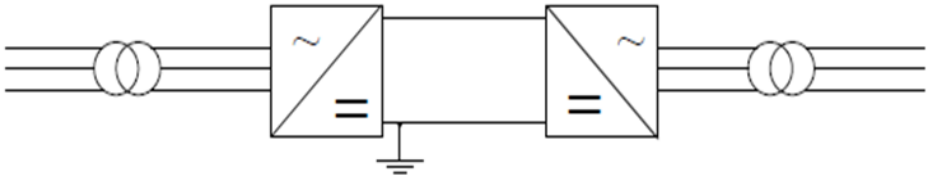


Figure 2. 5: Asymmetrical Monopole grid with metallic return.

(c) Symmetrical Monopole: Due to the symmetric nature of this topology, ac transformer is not subjected to dc voltage stresses, and during the pole-to-ground fault, the dc-side is not fed by a-side currents. In addition, this topology presented in Figure 2.6 has a higher cost compared to other monopolar since it requires two fully insulated conductors.

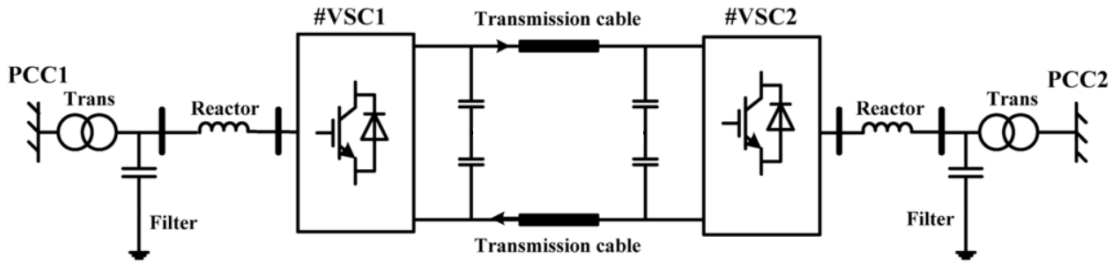


Figure 2. 6: Symmetrical Monopole

2.1.3.1 Multi-terminal HVDC

HVDC point-to-point converter station is the most common configuration, either connected by undersea cables or overhead power lines [43]. Advances

in HVDC, such as the development of VSCs, introduced the key technology for the future bulk power transmission. Grid interconnection improves capacity, which is a core contributor to the security of supply. The benefits of interconnection capacity include the following [44]:

- Increased capacity reserves and improves reliability.
- Cost-cutting in new generation units.
- Organising maintenance schedules.
- Supply security and diversified generation mix.
- New plant siting and environmental dispatch.
- The market potential will be increased.
- Load diversity will be increased, and the load factor will be improved

MTDC technology shown in Figure 2.7 using VSCs brought flexibility in the integration of large-scale renewable energy sources [45] and transmission network connection due to its capability of independent power control for both active and reactive power, black-start and ac voltage support (which may be weak). However, the protection of MTDC remains an unresolved issue. When the fault occurs in the MTDC system, only a faulted part should be cleared and isolated using a dc circuit breaker. There are several methods that have been proposed for MTDC protection, which still not reliable, they have drawbacks such as high on-state losses and lack of speed [30, 46]. Depending on the number of converter terminals, a good understanding of the transient currents and voltages is required for designing a reliable protection system.

Several MTDC projects are completed, and others are in advance stages in the world. MTDC-VSC Nan'ao Island in China was successfully commissioned in 2013, operating at 110/166 kV using MMC topology. Zhoushan archipelago in China consists of five converter terminal rated at +- 200 kV (MMC) interconnects five islands to meet up with the increasing power demand. Zhang-Bei is designed to supply clean power in Beijing from renewable sources such as hydro, wind, and solar power. Phase 1 is expected to have four terminals made up of half-bridge MMC. In India, an MTDC is still in the construction stage, and it is assumed to have three-terminal in the first phase using bipolar configuration [23]. To date, there are several VSC-MTDC

systems in operation, which are listed in Table 2.1, and others are still in the design and construction stage.

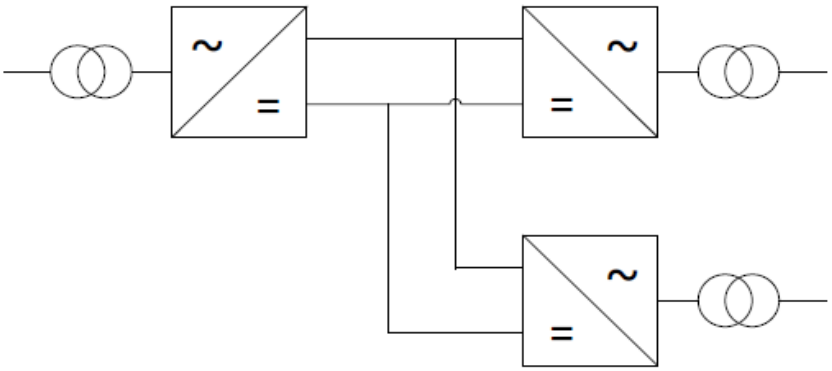


Figure 2. 7: Multi-terminal HVDC transmission system

Table 2. 1: List of Multi-Terminal VSC-HVDC Based (MTDC) System Projects [47]

Names/ Connection	No. of Terminals	Converter Type	Rating	Year
Zhangjiakou DC grid Demo Project	4	VSC	±500kV/3000 MW	2018
South-West Link	3	VSC	±300kV/1440 MW	2018
Tres amigas superstation	3	VSC	±345kV/750 MW	2015
Zhoushan MTDC Interconnection	5	VSC	±200kV,100/100 /100/300/400 MW	2014
Nao'ao MTDC	4	VSC	±160 kV, 200/100/50 MW	2013
Shin Shinano3 terminal VSC-B2B	3	VSC	10.6kV/53 MW	1999

2.1.4 VOLTAGE SOURCE CONVERTER vs. LINE COMMUTATED CONVERTER

Table 2.2 provides a detailed comparison summary between VSC and LLC technology. The comparison focus on the most important aspect listed in the first column, such as fault capability, Controllability, Black-start capability, Power direction control, and on-state losses.

Table 2.2: Detailed comparison summary between VSC and LLC technology [37, 42, 48, 49]

CRITERIA	**VSC-HVDC**	**LCC/CSC-HVDC**
Based on	IGBT's with an anti-parallel diode	Thyristors
Installation and operation time	Lesser time compared to LCC	More time compared to VSC
Physical size	Small compared to conventional HVDC	Larger than VSC-HVDC
Multi-terminal-HVDC	Suitable for multi-terminal-HVDC	Challenging due to the polarities of voltage
AC system	Weak AC network may be connected	Requires a strong AC network
Reactive Power	Not needed	Consumed and required
Reversal capability	Respond fast for power flow reversal	Limited power reversal capability
Commutation	Self-commutated	Line-commutated
Terminals Limits	No limits	Three terminals
Black-start capability	Available	Not available
Load types	Passive and active loads	Active loads
Harmonics	Lower AC filtering	Higher AC filtering
Controllability	Capable of controlling active and reactive power independently	Only active power can be controlled
Power direction control	By currents polarity	By DC voltage polarity
Technology	Still at its infancy levels	Fully matured
DC cables	Less expensive cables are used, and lightweight extruded cables	During power reversal, a cable must be able to withstand fast voltage polarity
On-state losses	Moderate	low
Fault capability	During dc side fault, the fault current will continuously feed the fault through anti-parallel diodes. The diode conduction can be stopped by opening the circuit breakers.	The fault currents increase can be stopped by control of the firing angle. This prevents the fault current from causing damage to the system.
Reactive power supply	No need for reactive power supply	Need a reactive power supply

2.1.5 VSC-HVDC Converter Station Components

The components of a typical VSC-HVDC transmission system is shown in Figure 2.8 and will be explained in the following:

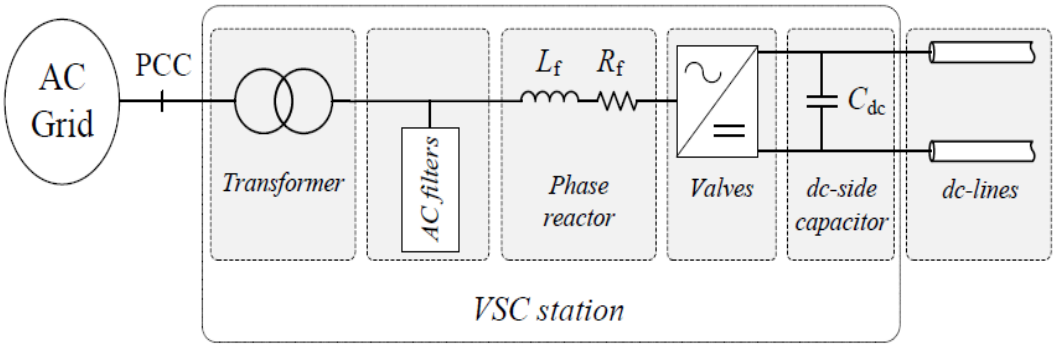


Figure 2. 8: Overview of VSC-based HVDC transmission system.

AC source unit

Generally, the AC grid is represented by three-phase lines, which are 120 degrees apart with series impedances. The ac source is represented as an ideal voltage source since the main focus is on the HVDC grid. The grid is considered to be perfectly stiff as it's not taking harmonic disturbances and Thevenin impedance into consideration. However, this assumption is not realistic in practice, especially when renewable sources are such as wind farms integration [50].

VSC-HVDC Converter (Valves)

The VSC converter is made up of switching devices such as IGBTs with anti-parallel diodes, and they can be operated in on and off position. The number of series-connected switches required to withstand the converter rating can be increased to offer a suitable redundancy if any unexpected failure occurs in some switches [51].

AC- side transformer

A three-phase power transformer is used to step-up/step-down the voltage to a suitable level for the converter station. An ordinary power transformer can be employed, and it also provides galvanic isolation between the dc side and the

ac grid. The transformer can be subjected to both AC voltage stresses, which are normally low and DC stresses.

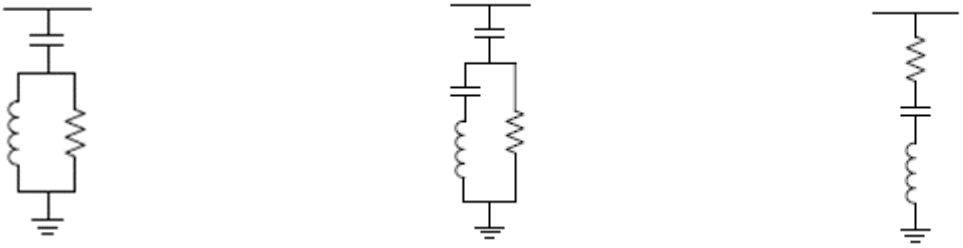
AC Filters

AC filters are mainly used for limiting harmonics of the converter voltages and currents, which can be harmful to the entire system. Filters are placed between the transformer and the converter. The components of the filter include capacitor, inductor, and resistor, as shown in Figure 2.9 (a-c) and can be calculated using equations [27]:

$$R = \frac{q}{\omega_0 C} \tag{2.1}$$

$$L = \frac{1}{C\omega_0^{\,2}} \tag{2.2}$$

$$C = \frac{Q_{shunt}}{2\pi f V^2_{\,n}} \tag{2.3}$$



(a)High-pass filter (b) C-type High-pass filter (c) Single tuned filter

Figure 2. 9: AC filters.

Where C = is the capacitance of the filter, Q_{shunt} = shunt reactive power, f = switching frequency, ω_0 = the tuned resonant frequency, V_n = the rated voltage, R = the resistance, q = quality factor and L = the inductance

Phase Reactor

Generally, phase reactors are connected on the VSC-HVDC side, and it plays an important role in a converter. Its purpose is to allow independent and continuous control of reactive and active power, and this is done by controlling the voltage drop and control the current flow across itself. The phase reactor also works as a filter for the harmonic currents generated by the converter [52].

Moreover, fast changes in polarity, which are the results of valves switching, can be prevented, while limiting short-circuit currents. The selected size of the phase reactor determine the dynamics of the converter. The large phase reactor will produce smaller peak-to-peak ripples but will slow down the dynamics of the converter. Therefore, there is a tradeoff in the phase reactor sizing. The phase reactor parameter is selected to be $0.15pu$.

DC Capacitor

The main purpose of the capacitor is to operate as an energy-storing device so that power flow can be controlled and to allow a low-inductance path for the turn-off current. Also, it reduces the DC voltage harmonic ripples. The sizing of the capacitor is an essential component since it is a trade-off between control stiffness and capacitor lifetime, ripple tolerance, space restriction as well as the cost. In practice, the size of the dc capacitor as in equation (2.4) depends on the desired transient behavior, which is determined by the time constant, τ as explained in equation (2.5). Time constant is simply defined as the time required to fully charge the capacitors at the rated voltage level and rated power [50] [53].

$$C_{dc} = \frac{2 \times \tau \times S_n}{V_{dc}^{\ 2}} \tag{2.4}$$

Therefore,

$$\tau = \frac{C_{dc} \times V_{dcN}^{\ 2}}{2 \times S_N} \tag{2.5}$$

Where, τ = time constant
V_{dc} = rated voltage
S_N = rated power
C_{dc} = DC capacitor

2.1.6 Voltage Source Converter Operation Quadrants

VSCs have the ability to operate in all four quadrants of the P-Q circle, as illustrated in Figure 2.10, and independent control of reactive and active power can be achieved. P-Q circle outline the operating mode of the VSC for the direction of active power flow for inverter or rectifier operation and direction of reactive power flow for capacitive and inductive mode [54] [55].

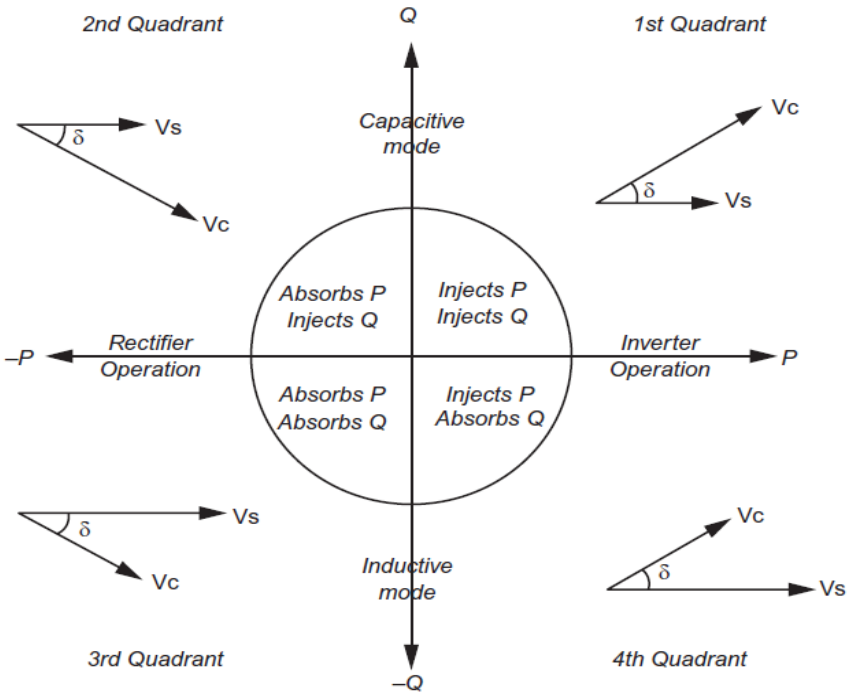


Figure 2. 10: P-Q circle diagram for the VSC converter [55]

2.1.6.1(a) Rectifier Operation of VSC

The direction of current flow determines the mode of operation of VSC as an inverter or rectifier. The phasor diagram in Figure 2.11 shows how rectifier mode is achieved in the VSC converter, the ac system voltage *Vs* leads the converter voltage *Vc* by an angle δ. Consequently, the active power will flow from the ac system to the converter, and the current flowing is considered positive.

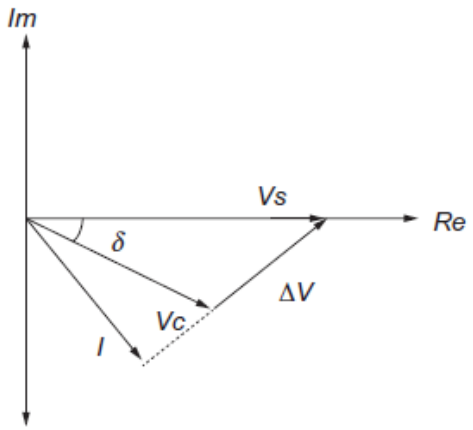


Figure 2. 11: VSC rectifier operation.

From the P-Q circle, the second and third quadrant falls under rectifier mode due to the lead of the ac system voltage over the output converter voltage. However, the second quadrant injects reactive power (capacitive mode) as the magnitude of *Vc* is much higher than *Vs*. The third quadrant absorbs reactive power (inductive mode) as the magnitude of *Vs* is greater than *Vc*.

2.1.6.1(b) Inverter Operation of VSC

The phasor diagram illustrated in Figure 2.12 shows the output ac voltage of the converter leading the ac system voltage by the angle δ, hence active power flows from the converter to the ac system, and the dc current becomes negative.

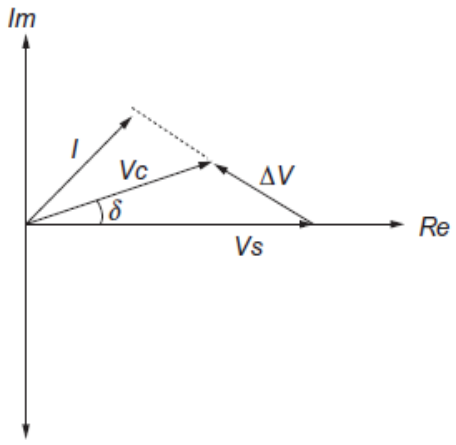


Figure 2. 12: VSC inverter operation.

The first and fourth quadrant falls under inverter mode. The first quadrant injects reactive power to the ac system, which explains the capacitive mode of inverter operation. At this point, the magnitude of the converter output is higher than the ac bus system. The latter explains the inductive mode of inverter operation, where ac bus voltage is greater than the converter output ac voltage [54].

During the operation of the VSC converter station, the maximum current $I_{\max}$ must not exceed at any given time. The right of way is given to transfer active power compared to reactive power flow. The maximum current capacity $\pm I_{\max}$ is limited by, I_d whereas I_q it is limited such that the total current does not exceed the rated current of the converter station as given in eq (0) [56] [57].

$$I_{rated} = I_{\max} \tag{2.6}$$

$$I_{q\max} = \sqrt{(I^2{}_{rated} - I^2{}_{d})} \tag{2.7}$$

Converter Configuration

VSC-based HVDC systems mainly utilize three types of converter configuration, namely: two-level converter, three-level neutral point clamped (NPC) converter, and modular multilevel converter.

2.1.7 VSC–HVDC Based on Two-Level Converters

The main circuit structure for a three-phase two-level topology shown in Figure 2.13 is the simplest and consists of 3 legs, each leg connected to one phase. Each leg has only two switches, which results in a small footprint. This topology output voltage has two levels [37]. This topology has been widely used in many applications at a wide range of power levels. Two-level converter synthesizes two-voltage levels -0.5*Vdc* and +0.5*Vdc*; they are robust, reliable in performance, and have a simple configuration [18] [58] [59]. The converter valves consist of IGBTs switches and anti-parallel diodes. For high power applications, a series connection of switches may be necessary.

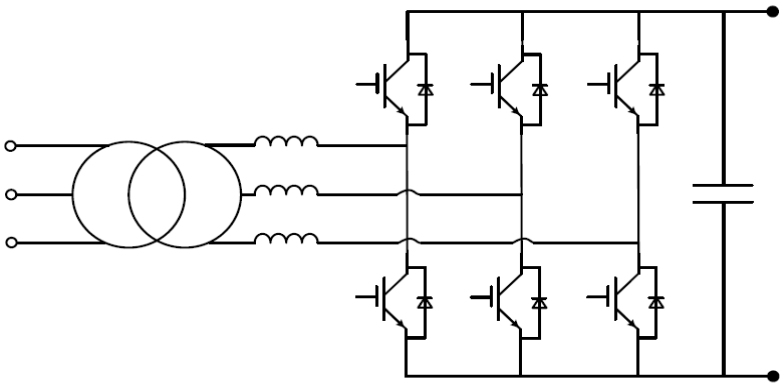


Figure 2. 13: Architecture of a two-level VSC topology.

The switching operation (turning on/off) of these switched depends on a gate signal, which is generated using pulse width modulation (PWM) technique, as seen in Figure 2.14. PMW is based on the comparison between reference waveform and a carrier waveform. When the reference waveform signal exceeds the carrier waveform signal, the switching device will be turn on and

vice versa. However, this will synthesize an output waveform with frequency harmonics. Therefore filtering equipment is required to filter out the harmonics. The typical range of switching frequency is between 1 kHz to 2 kHz is mostly used in two-level VSC converters [47].

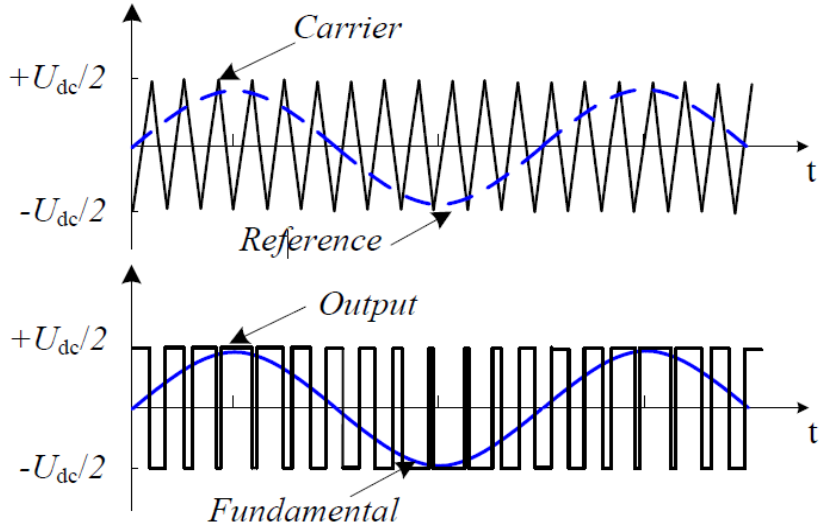


Figure 2. 14: PWM waveform.

Advantages:

- simplicity, reliability, complexity and performance.

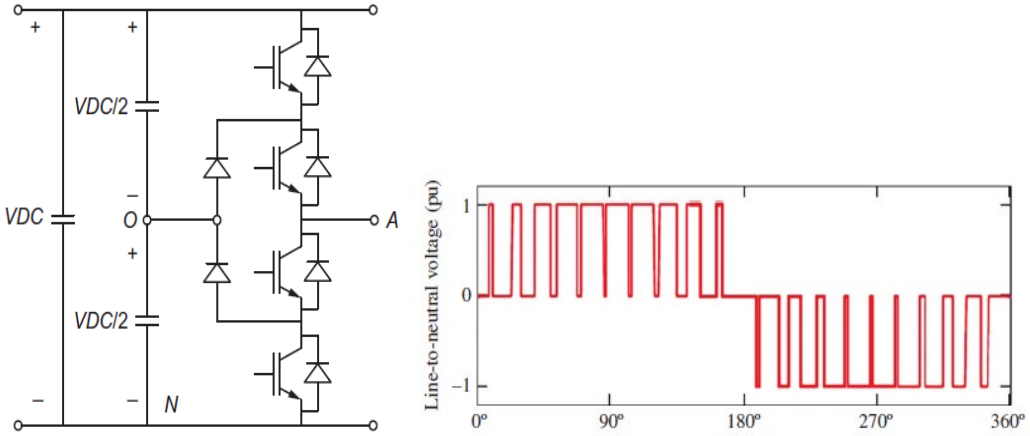
Disadvantage [60]:

- interfacing transformers require high insulation due to high dv/dt,
- higher switching losses
- Interference from electromagnetic

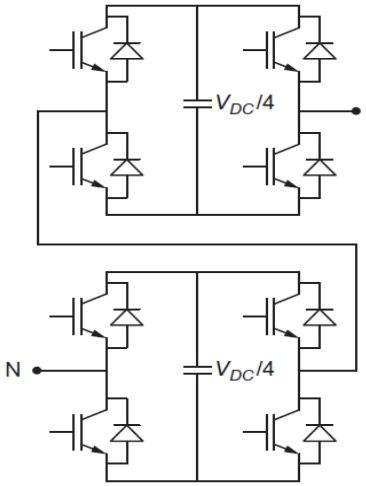
2.1.7.1 VSC–HVDC Based Multilevel Converters

Multi-level converters have a unique structure when compared to a conventional two-level topology, their structure enables them for high voltage and high power applications such as HVDC, flexible alternating current transmission systems (FACTS), and large electric adjustable speed motor drive (ASMD) [61]. A multi-level converter produces output voltage with more than two levels of voltage. Compared to two-level converters, a multi-level converter synthesizes improved sinusoidal voltage waveform output, which requires less filtering [62] with the help of PWM [63]. Figure 2.15 (a) shows a diode-clamped neutral-point-clamped three-level converter with output waveform. Three-level converter synthesizes 3-voltage levels -0.5Vdc, 0, and

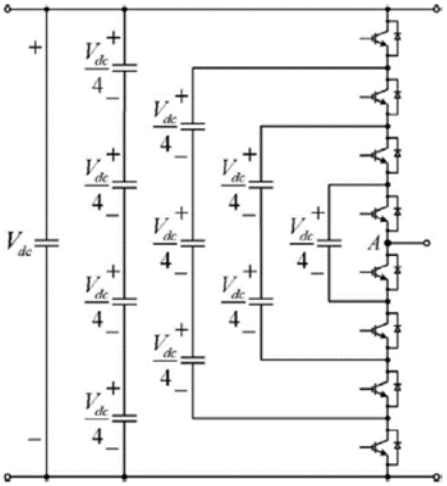
+0.5Vdc waveforms. The well-known multilevel VSC topologies are neutral-point-clamped (NPC), the cascaded H-bridge (CHB), the flying capacitor, and MMC shown in the follows Figure 2.15 (a-d) [64] [65] :



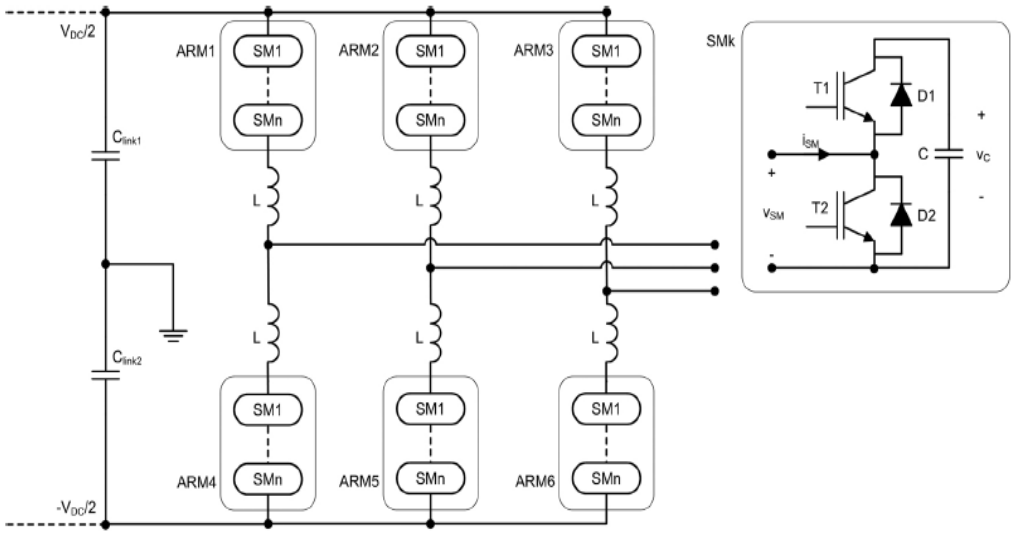
(a) Neutral-Point-Clamped converter

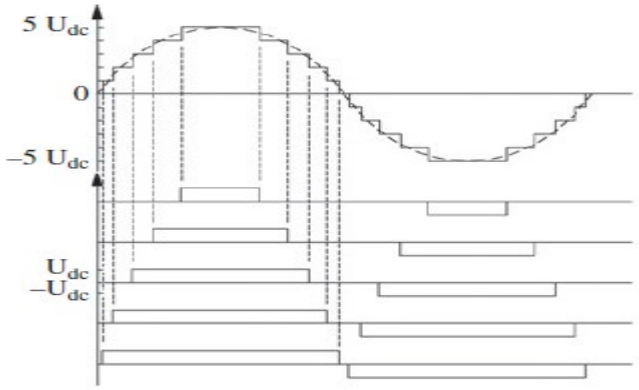


(b) The cascaded H-bridge



(c) The flying capacitor converter





(d) MMC converter

Figure 2. 15: Multilevel converter topologies (a) NPC, (b) CHB, (c) FC (d) MMC.

NPC Multilevel VSC

Advantages [66]

- The output rating is increased.
- The voltage across the IGBT switches is reduced to half of the dc bus voltage.
- The output voltage waveform has reduced harmonics for the same switching frequency.

Disadvantage [67]

- The control is complex.
- More clamping diodes are required for a series connection in the higher level application.

H-bridge Multilevel VSC

Advantages [68, 69]

- Requires less number of components than the FC and NPC converter topologies for the same number of voltage levels.
- The modular structure is made up of identical H-bridges, which makes it easy to package the modular circuit layout.

Disadvantages

- Each stage of H-bridges requires an isolated dc power supply.

Flying Capacitor Multilevel VSC

Advantages [70, 71]

- It has the ability to control flying capacitor voltages using redundant state selection regardless of voltage levels (higher than three levels).
- It cancels the presence of clamping diodes.
- Voltage levels can be easily improved than the NPC topology.

Disadvantages [61]

- Capacitors bank size increased.
- The requirement of pre-charging circuitry.

MMC Topology

Advantages [15]

- There a significant reduction in the need for ac-side and dc side filtering due to harmonic cancelation between the submodules (SMs)
- MMC has easy scalability.
- There is less stress in the semiconductor.
- The topology reduces the distribution of capacitive energy between several capacitors.

Disadvantage [15]

- There is an increase in the number of drivers and modules.
- The complexity in controls of MMC due to presence of circulating three currents that flow between each phase and dc bus.
- There is an increasing number of signals to be controlled, such as SM voltage feedback and module trigger.

2.1.8 Pulse Width Modulation Techniques

Commutation of converter switches in VSCs can be achieved by applying on or off signals at the gate of IGBTs. By turning signals on or off, AC systems output voltage magnitude and phase angle can be controlled relatively [ester]. A signal such as Sinusoidal PWM, Space vector modulation, and Selective harmonic elimination PWM is generated for modulation purposes in the VSCs.

2.1.8 (a) Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal PWM technique is the simplest and commonly used for VSCs, and it produces its output waveform by comparing high-frequency triangular

waveform, which is known as a carrier with the sinusoidal waveform which is known as fundamental/reference waveform as shown in Figure 2.16. The comparison of triangle frequency waveform and the fundamental waveform is done in such a way that when the fundamental waveform is higher than the carrier waveform, the switch is turned on. Likewise, the switch will be turned off when the fundamental is lower than the carrier waveform [5]. The elimination of even harmonics and generation of symmetrical 3-phase voltages can be done by always making the carrier frequency to be an odd multiple of 3 as this offers half and quarter symmetry. The ratio of the switching frequency f_{sw} and reference frequency f_r is called frequency modulation index m_f: [9]

$$m_f = \frac{f_{sw}}{f_r} \tag{2.8}$$

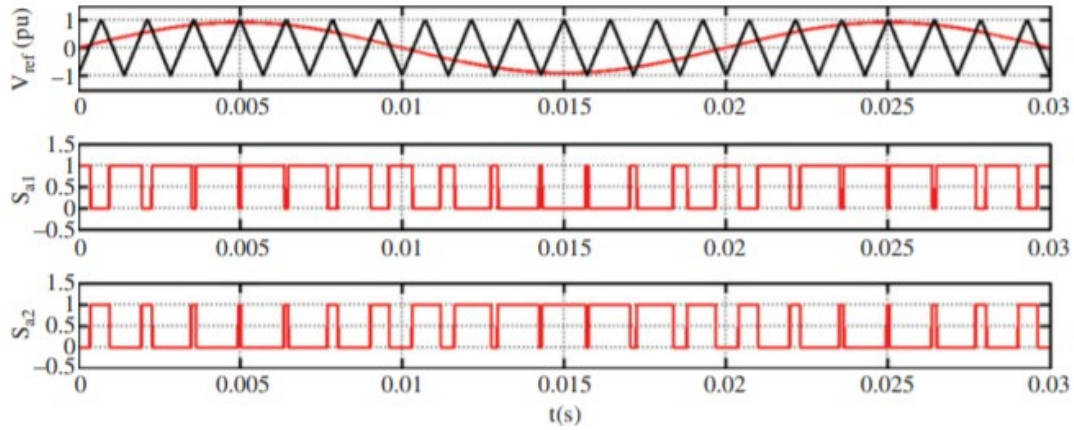
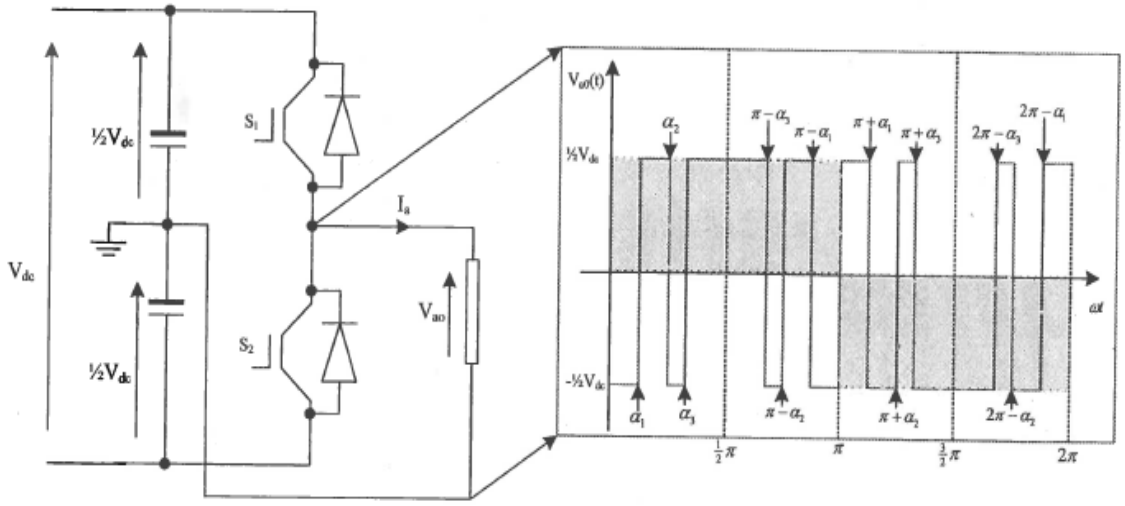


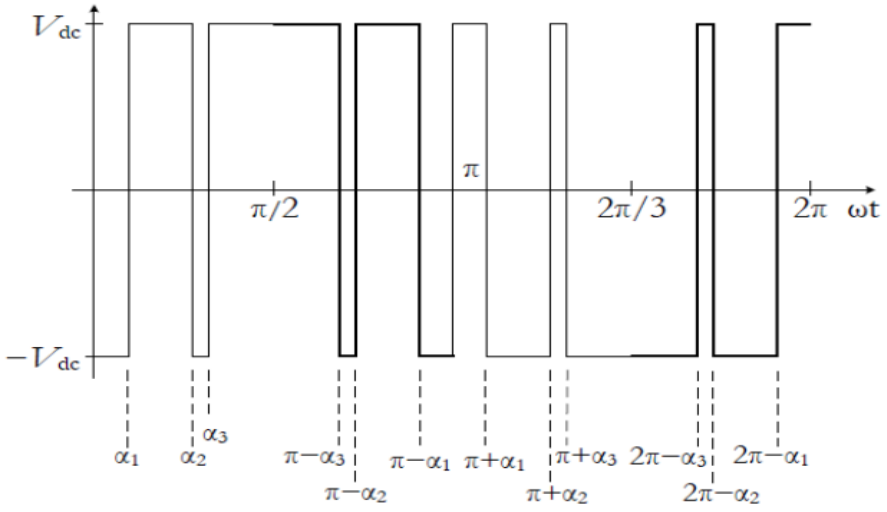
Figure 2. 16: Single-phase waveform of SPWM with generated gating signal.

2.1.8(b) Selective Harmonic Elimination (SHE PWM)

Phase voltage output switching angles is identified by SHE-PWM through setting the magnitude of the phase voltage and stipulating the voltage harmonics to be eliminated. This results in fundamental phase voltage being chopped into a small pulse with notches located at the angles α_1, α_2 and α_3. Also, angles α_1, α_2 and α_3 are selected to eliminate pre-determine harmonics [62]. Figure 2.17 (a) illustrates how SHE-PWM form gating signals for the switching of three-phase two-level VSC. From Figure 2.17 (b), the first angle (α_1) is used for setting the fundamental magnitude, and the rest of the angles are employed to eliminate the defined low-order harmonics.



(a)



(b)

Figure 2. 17: SHE-PWM form gating signals for the switching of single-phase two-level VSC.

SHE is advantageous in improving the dc voltage utilization; however, this depends on the number of harmonics to the removed. Also, it presents the ability to control the fundamental voltage without producing unwanted switching instances and to target pre-determined harmonics, which leads to low switching losses. On the other hand, SHE requires a look-up table to keep the switching angles and offline calculations. Moreover, practical application is difficult [2].

However, these PWM strategies that are discussed are for a basic two-level VSC that has two converter switches each leg.

2.1.8(c) Space Vector PWM (SVPWM)

The space vector modulation (SVM) theory was proposed in the mid1980s [62], and it is widely employed in low and medium voltage drives systems, and now it is well established. This modulation technique is assumed to have significant advantages over a traditional carrier-based modulation technique such as easy digital implementation, the possibility of optimizing the switching sequences and improve dc-link voltage utilization. The method used for the calculation of the voltage vector for two and three-level can also be extended and applied for multilevel converters. However, its application is limited to motor drives, with small chances to be applied in grid-connected converters. The development of SVM is suitable for a three-phase balanced ac system such as the motor in a drive system, but for unbalanced applications, this technique introduces substantial complexity to the modulation process. Moreover, this technique requires high switching frequency to synthesize high-quality output current and voltage. Using Clark's transformation in Figure 2.18, phase-leg voltages produced by eight possible switch combinations can be transformed into the stationary reference frame a-b

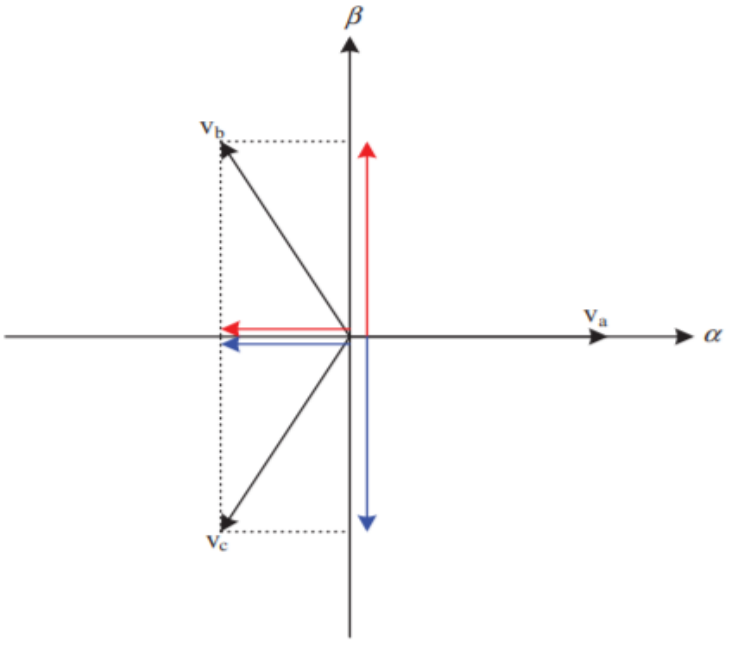
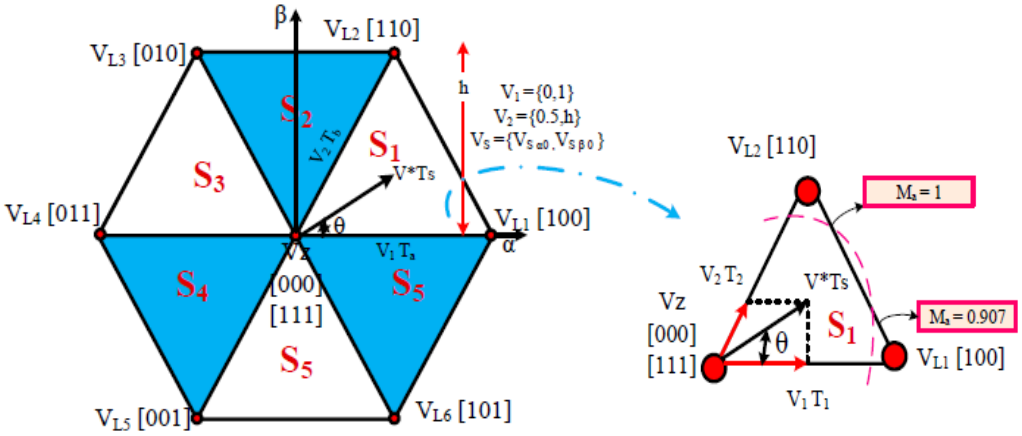


Figure 2. 18: Three-phase variables transformation to $\alpha - \beta$ plane.

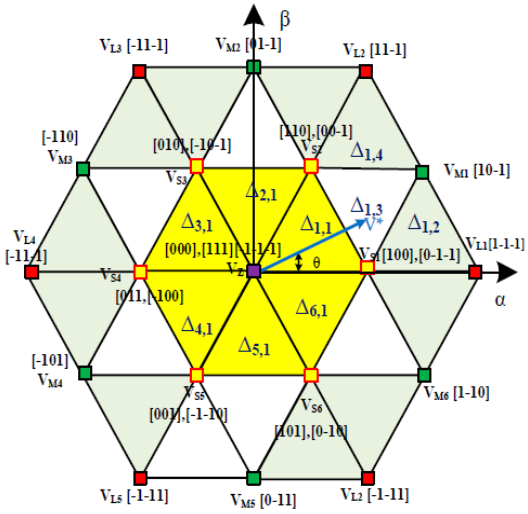
The converters phase leg voltages (*Va0, Vbo, and Vc0*) are transformed to their equivalent, assuming phase voltage *Va* is aligned with *a* given by equation (2.9)

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix} \tag{2.9}$$

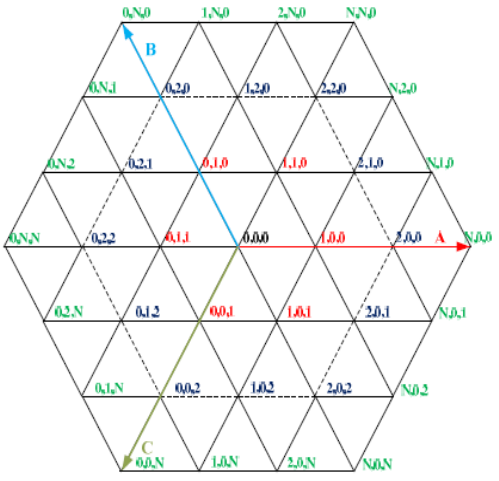
The space vector plane for a two-level converter is shown in Figure 2.19 (a); the diagram consist of six sectors, labeled 1 to 6 and figure b generation of reference voltage in the first sector. SVM for 3-level NPC is shown in Figure 2.19 (b) and for N-level converter is illustrated in Figure 2.19(c) where each connection point denotes a specific state of the three-phase voltages of the converter.



(a) space vector plane for a two-level converter



(b) SVM for 3-level NPC



(c) SVM for N-level converter

Figure 2. 19: Space voltage vectors in different sectors for two-level and multilevel topologies.

2.1.9 Sinusoidal Pulse Width Modulation (SPWM) Block

2.1.9.1(a) Multilevel Carrier-based PWM

Most sinusoidal pulse width modulation (SPWM) for multilevel VSC is derived from the carrier disposition strategies, which were first presented by Carrara et al. [72]. For a multilevel NPC converter with *N*-level, the triangular carriers *N-1* with the same amplitude and frequency are such that they fully occupy the band over the range of $+V_{dc}$ to $-V_{dc}$. The reference signal for each phase is then compared to these carrier signals to produce gating pulses which are used for converter switching. The modulation index for the various multicarrier modulation technique is defined by equation (2.10) [73] [74]:

$$m_a = \frac{A_0}{\frac{m-1}{2} A_{c(p-p)}} \tag{2.10}$$

Where: A_0 and $A_{c(p-p)}$ are the carrier signal and amplitude of the reference signal, m_a is the number of levels.

The carrier disposition PWM strategies with differing phase relationships between the carriers can be categorized as follows:

2.1.9.1(b) Phase Disposition (PD)

All carrier signals in phase disposition are in phase [72] [73] [75] [76] as shown in Figure 2.20

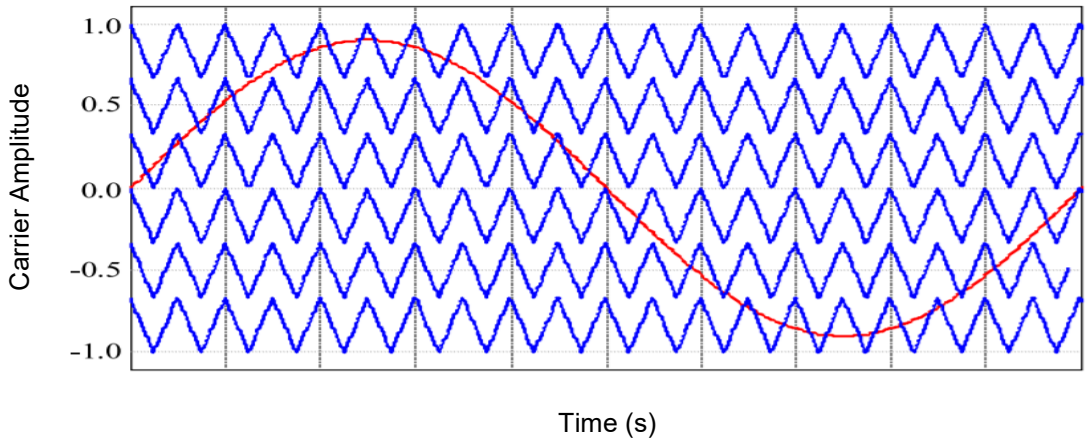


Figure 2. 20: Carrier wave and reference wave arrangement of PD method.

2.1.9.1(c) Alternative Phase Opposition Disposition (APOD)

Figure 2.21 shows the arrangement of an alternative phase opposition disposition method, where each *N-1* carrier signal is displaced from each other by 180 degrees alternately [72] [75].

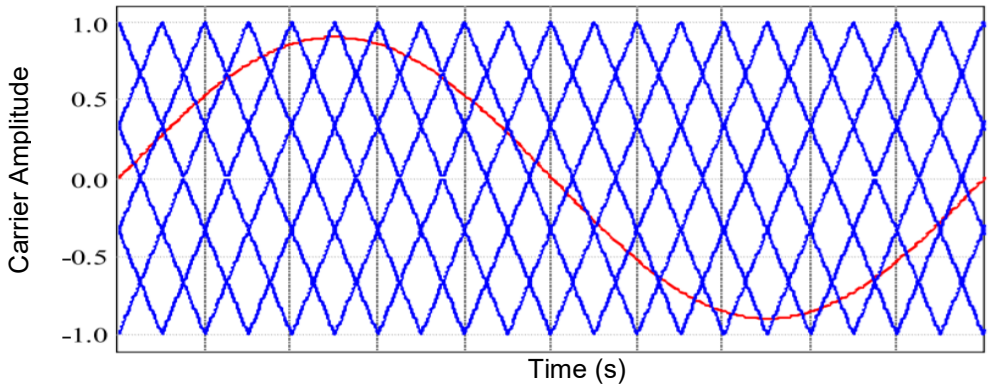


Figure 2. 21: Carrier wave and reference wave arrangement of the APOD method.

2.1.9.1(d) Phase Opposition Disposition (POD)

With this method, all the carrier signals above the zero reference value are in phase, the carrier signal below the zero references is in phase but are 180 degrees shifted from those above zero [72] [73] [77] [75] as shown in Figure 2.22.

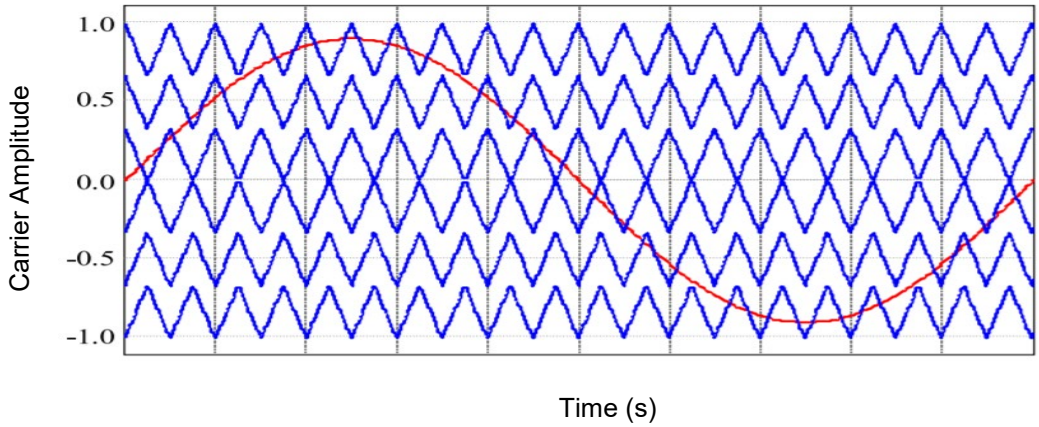


Figure 2. 22: Carrier wave and reference wave arrangement of the POD method.

2.2 CONTROL STRATEGY OF VSC

One of the advantages of VSC-HVDC over conventional HVDC is the ability to fully control the switches. When it comes to the controls of VSC, vector control and direct control are mainly two control techniques that are well developed and being used. Although direct control technique is easy to implement and shows positive results when it comes to fast dynamic response, it was concluded that the vector control technique performs better due to lower currents distortions, higher overall efficiency, and higher grid power factor. One of the primary disadvantages of vector control is the presence of low-frequency resonance when the VSC is connected to a weak network. The difference in phase voltages between the ac side at the point of common coupling (PCC) and a point where the converter station is connected is accountable for active power transfer. The power will flow from the ac side to the dc side of the load angle is positive and vice versa. The power flow can be expressed by equation (2.11). Reactive power will be controlled by the highest magnitude of the ac voltage using equation (2.12) [78]. Figure 2.23 shows the basic operation of the VSC-HVDC based transmission system, considering the voltage source connected to the ac system using filtering equipment [50].

$$P = \frac{V_{ac} \times V_c}{X} \times \sin\delta \tag{2.11}$$

$$Q = \frac{V_{ac}\cos\delta - V_c}{X} \times V_c \tag{2.12}$$

Where δ = load angle between the voltages

V_{ac} = Grid voltage

V_c = Converter side voltage

X = Interconnecting reactor

P = Active power

Q = Reactive power

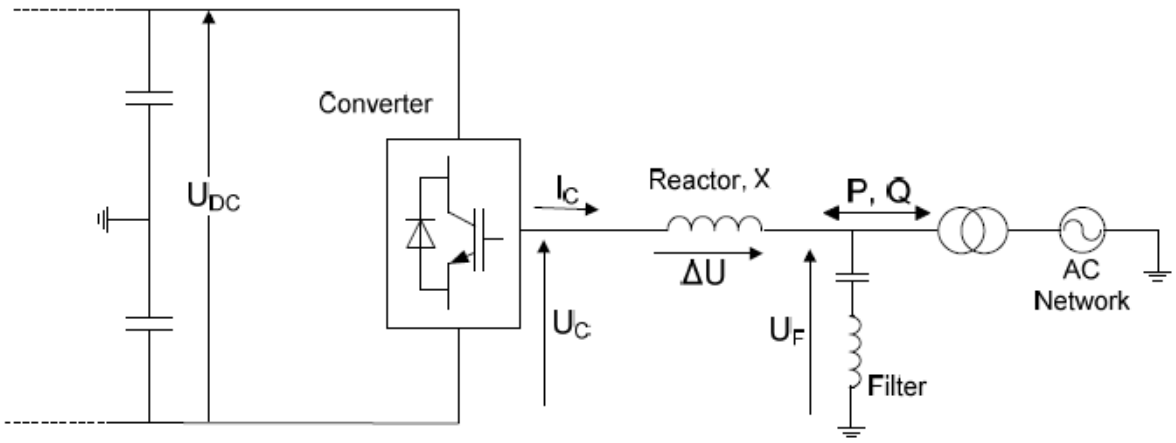


Figure 2. 23: Single-line diagram for VSC basic operation.

From Figure 2.23, the fundamental frequency output voltage of a VSC is given by equation (2.13)

$$U_c = \frac{1}{2} m_a U_{dc} \sin(\omega t + \theta) \tag{2.13}$$

Where, m_a = modulation index,

θ = phase shift

U_c = is the output voltage

ω = fundamental frequency.

$$m_a = \frac{\sqrt[2]{V_d^{\,2} + V_q^{\,2}}}{U_{dc}}$$

$$\theta = \tan^{-1}\left(\frac{V_q^{\,2}}{V_d^{\,2}}\right)$$

The overall vector control structure of the VSC-HVDC is illustrated in figure 2.24. Since not all controllers can be used at the same time, each side of the converter can either use dc voltage control or active power control. For the inner current controller, each of these controllers produces a reference value. The choice of various types of controllers to measure the converter current's reference values will depend on the application and may require some advanced analysis of the power system.

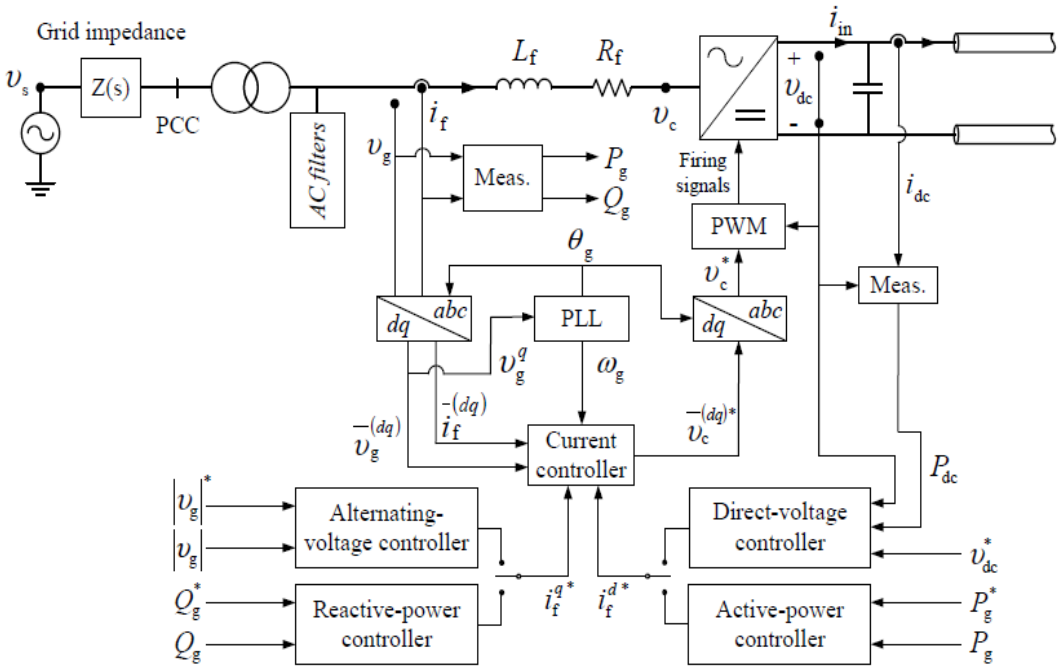


Figure 2. 24: Main-circuit and control block diagram for a VSC converter using vector control.

2.2.1 Phase Lock Loop (PLL)

The phase lock loop (PLL) is practically applicable in many electronics pieces of equipment apart from power grids. It is also used in fields like communication where they use it for phase-locking existing signal, and it is using its internal oscillator. Generally, when a VSC converter is connected to an ac system, the PLL is used to ensure accurate synchronization to the ac system by providing frequency input of the filter bus voltage and phase angle to the control system of the VSC. PLL plays a significant role in the system operation when using the d-q reference frame [79]; under fault conditions, PLL has a great impact on transient performance [80]. The software structure is shown in Figure 2.25. The basic structure of PLL includes three portions, as illustrated in Figure 2.26. In the diagram, the first block is a phase detector (PD, a loop filter (LF), and a voltage-controlled oscillator (VCO). Basically, the phase detector compares the desired signal and the signal created by the VCO in order to determine their phase difference and output value, which is proportional to this difference. As shown in the figure, the signal from the PD is passed into a low-pass filter represented by the proportional-integrator (PI) components controller. From LF, the output signal is fed into VCO as an input

signal in order to create the desired signal (normally 60Hz or 50Hz) to match that of the input signal of the PLL [81].

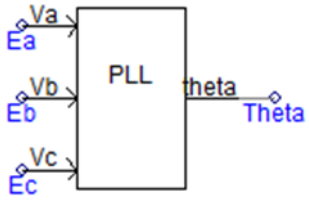


Figure 2. 25: PSCAD PLL control block.

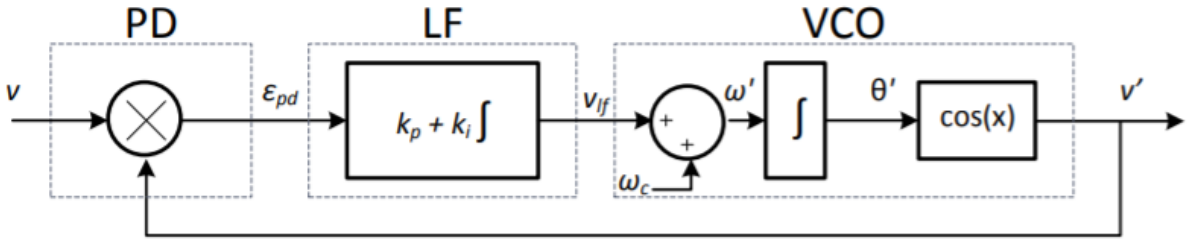


Figure 2. 26: Block diagram of PLL.

2.2.1.1 Direct control strategy

In this control, active power is associate with reactive power such that any deviation in an active power will immediately affect the reactive power. Thus independent power control is not achieved using direct control [78].

2.2.1.2 Vector control strategy

The reason vector control is preferred than direct control is that it has an ability to control instantaneous active power and reactive power independently in the $d-q$ synchronous reference frame. The $d-q$ representation is achieved by park transformation where vector quantities of ac currents and voltages are transformed into a rotating signal, as seen in Figure 2.27. The transformation of coordinates from three-phase stationery is determined by Clark to transform. The three-phase vectors are transformed into $\alpha-\beta$ stationary coordinates to the $d-q$ rotating vectors [82] [53].

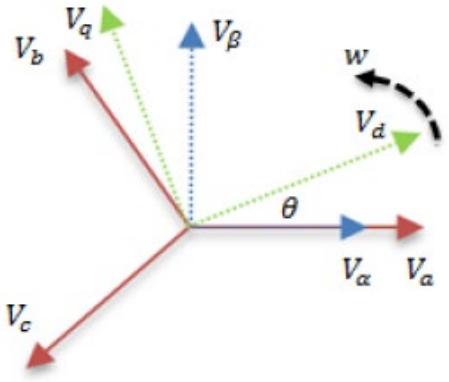


Figure 2. 27: The $\alpha - \beta$ and $d - q$ system transformation.

It comprises of three control loops, which are known as phase lock loop (PLL), outer control loop, and inner current control loop. The outer control loops are used to control several parameters, such as the AC voltage, DC-link voltage, reactive power, and active power. The architecture of vector control is shown in Figure 2.28 [50]. Figure 2.29 shows the software structure of the transformation block.

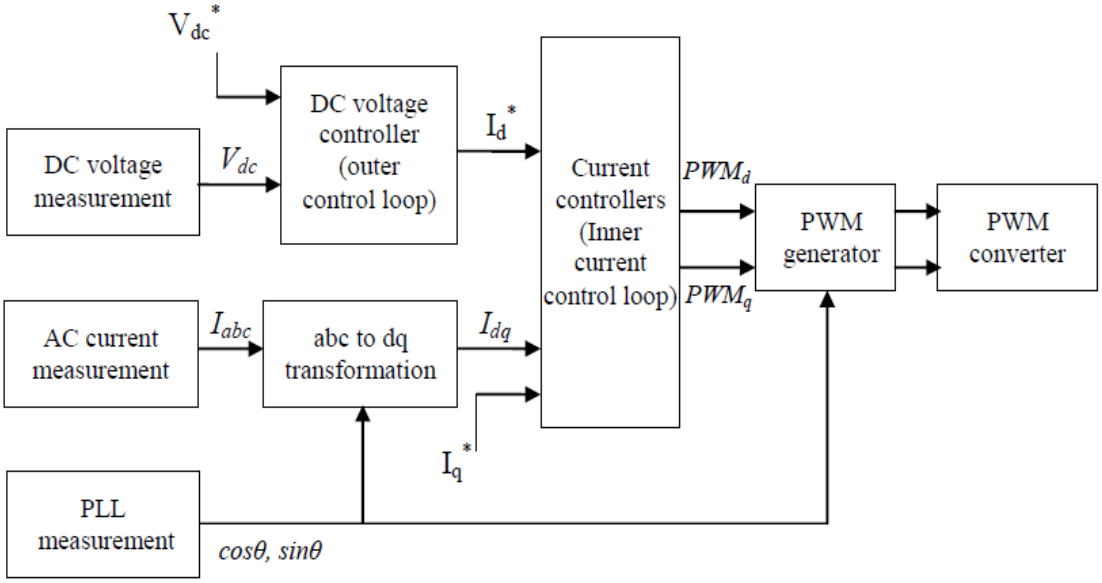
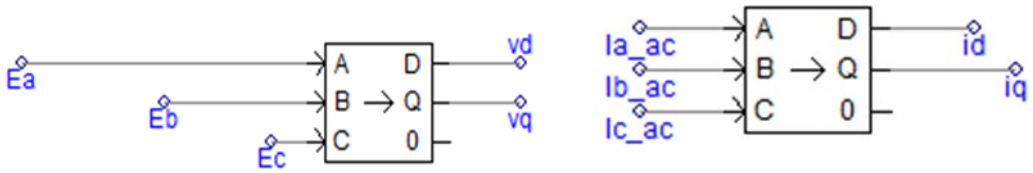


Figure 2. 28: Block diagram of the vector control system [83].



(a) (b)

Figure 2. 29: D-Q transformation block representation on PSCAD.

2.2.1.3 Inner Current Controller

The feedback loop of the inner current controller (ICC) is shown in Figure 2.30 and the ICC block diagram shown in Figure 2.31. is used to track the reference currents i^*_d and i^*_q which are set by the outer controller through the fast proportional-integral (PI), and the output signals generated are two voltage references (i.e., V_d and V_q) for the converter and the controller output is developed based on equation (2.14-2.15) [84] [53].

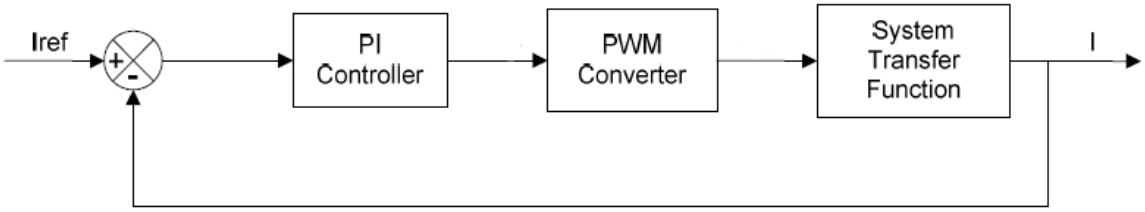


Figure 2. 30: Inner current loop control block diagram

$$U_d = \left(k_{pi} + \frac{k_{ii}}{s}\right)\left[i^*_d - i_d\right] + V_d + (\omega L) \times i^*_q \qquad (2.14)$$

$$U_q = \left(k_{pi} + \frac{k_{ii}}{s}\right)\left[i^*_q - i_q\right] + V_q + (\omega L) \times i^*_d \qquad (2.15)$$

Where, k_{pi} = proportional gain

k_{ii} = integral gain

ωL =

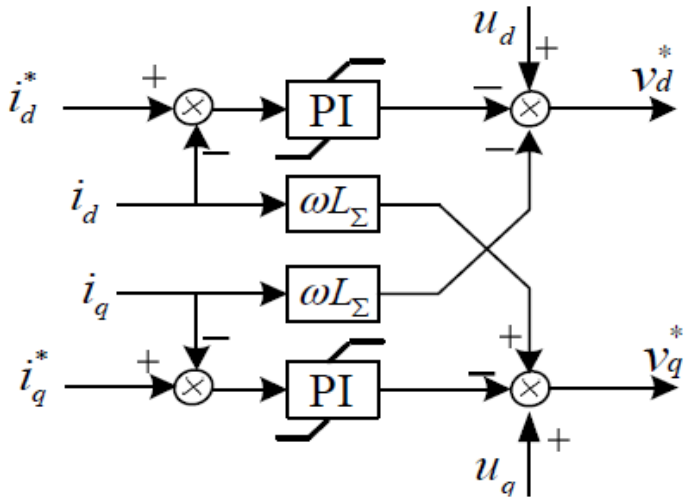


Figure 2. 31: The basic structure of the inner current controller.

2.2.1.4 Outer Controller

The outer controller is used to provide a current reference signal for the active current controller. This controller usually controls active and reactive power, dc voltage, and ac voltage. The feedback loop, which is the combination of a PI regulator and open-loop, is employed for all the controllers in order to annul steady-state errors to achieve more accurate signals.

2.2.1.4 (a) Active Power Control

The active power controller is responsible for regulating the power exchange at the common bus to match the reference given value by adjusting the i^*_d signal. The output of this controller serves as input in the current controller. Then, the limiter function is used after the output of the controller in order to limit the magnitude of the VSC-HVDC current to the maximum limit. The instantaneous real power absorbed from the AC system will be expressed by equation (4), and a basic structure of this controller is shown in Figure 2.32.

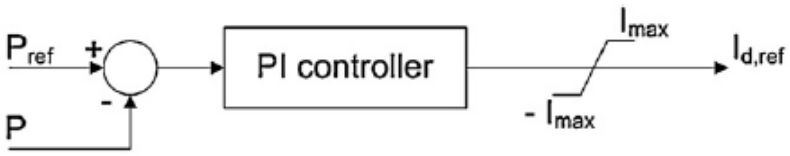


Figure 2. 32: The basic structure of the active power controller.

According to the conservation of energy law, the active power transferred in the MTCD-HVDC system satisfy equation (2.16)

$$P_1 + P_2 + P_3 + P_4 + P_5 = 0 \tag{2.16}$$

2.2.1.4 (b) AC voltage Control

AC voltage control: The amplitude of the ac voltage at the common bus is regulated by the ac voltage controller, which is shown in Figure 2.31 such that a given reference value is equal to the measured value by modifying the i^*_q reference signal. Thus, this controller governs the converter terminal to generate the required amount of reactive power so that the voltage at the common bus matches the given reference value

2.2.1.4 (c) Reactive Power Control

Reactive Power Control: The reactive power injection in the power system can be independently controlled in every converter terminal. The reactive power exchanged at the common bus matches the reference value given by modifying i^*_q . The instantaneous reactive power absorbed from the AC system will be expressed by equation (3), and a basic structure of this controller is shown in Figure 2.33.

Figure 2. 33: The basic structure of the reactive power controller.

2.2.1.4 (d) DC Voltage Control

The proper performance of MTDC grids relies on essential operational tasks such as dc voltage control, power-sharing, and active power control. A power balance can be guaranteed between all the interconnected nodes if dc voltage is well controlled in the grid [85]. Real-time communication cannot be used as primary control due to the distance between the converter stations. Local control is preferred for each station [86]. Voltage control in the MTDC grid can be achieved by three main strategies, namely: voltage margin, voltage droop, and master-slave strategy [87]. DC grid stability depends on proper control of

dc voltage as any power imbalance within the grid can cause dc under- or overvoltages. During normal and abnormal operating conditions, dc voltage should be restricted within a small variation range in order to protect network equipment such as dc cables, converter semiconductor and passive devices from stress in case of higher dc overvoltages. DC under-voltages can impact the network negatively by increasing the system's power losses and converter's ability to synthesize the required voltage at the ac terminal. Failure to produce the required ac voltage leads to the loss of controllability of the system. Controlling voltage of the dc grid to a narrow range and define its minimum and maximum limits are one of the solutions to avoid consequences that may arise due to a sudden change in the operating condition. Figure 2.34 shows DC voltage Close loop control Figure 2.35 show the basic structure of a dc control using a fast PI controller. Droop control methods include voltage-power (V-P) droop, voltage-current (V-I) droop, and voltage droop with different dead-bands and limits. However, only V-I and V-P will be discussed in the literature

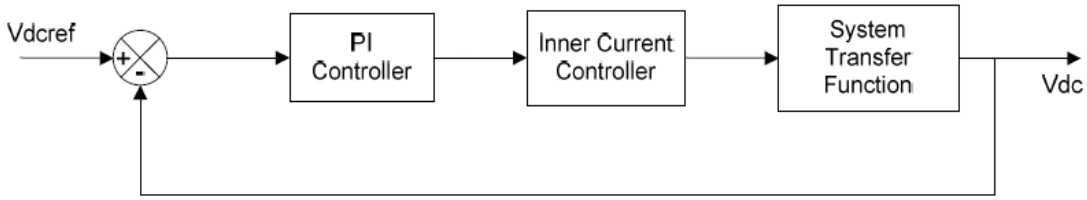


Figure 2. 34: DC voltage Close loop control block diagram.

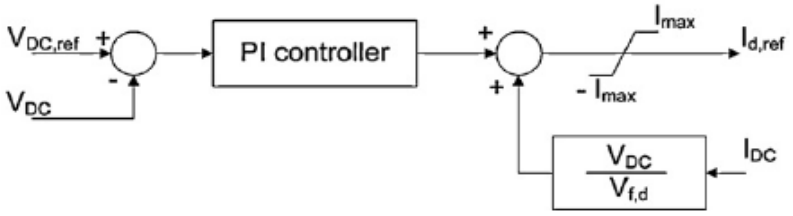


Figure 2. 35: The basic structure of the dc voltage controller.

2.2.1.4.1 (a) Master-Slave Method

The application of master-slave dc control in the MTDC system illustrated in Figure 2.36 dedicate only one converter to regulate the dc voltage in the grid while other converter stations control the power [86]. This method is practically

implemented in the Nan'ao MTDC system [88]. This method provides highly operation accuracy; however, this method is highly dependent on remote information and fast communication. Consequently, this method suffers from low reliability if dc voltage control is lost [89]. Issues such as instability caused by the failure of the master converter make this method unsuitable for MTDC. Moreover, the performance of this method depends on the stiffness of the ac grid to ensure the fast conditioning of the dc grid and avoid adverse effects on the ac grid [88].

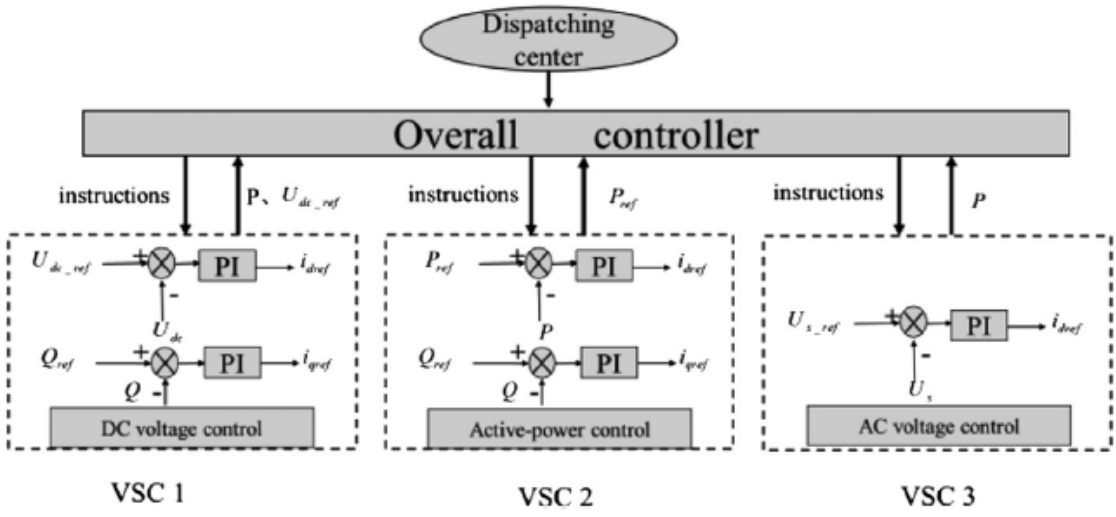
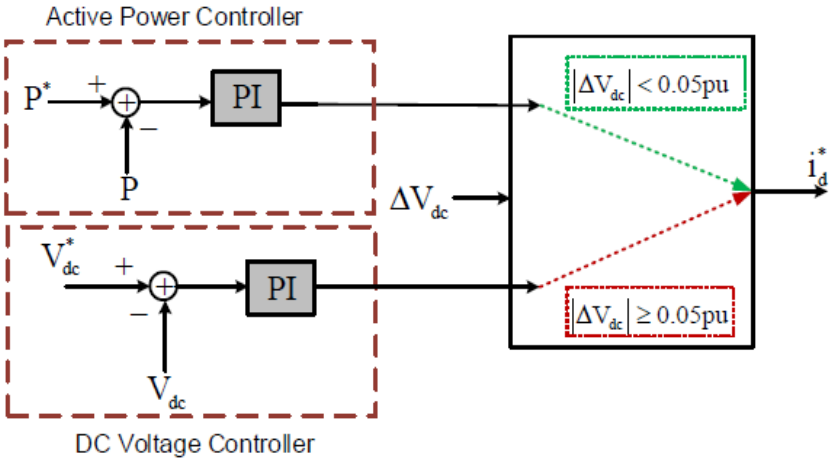


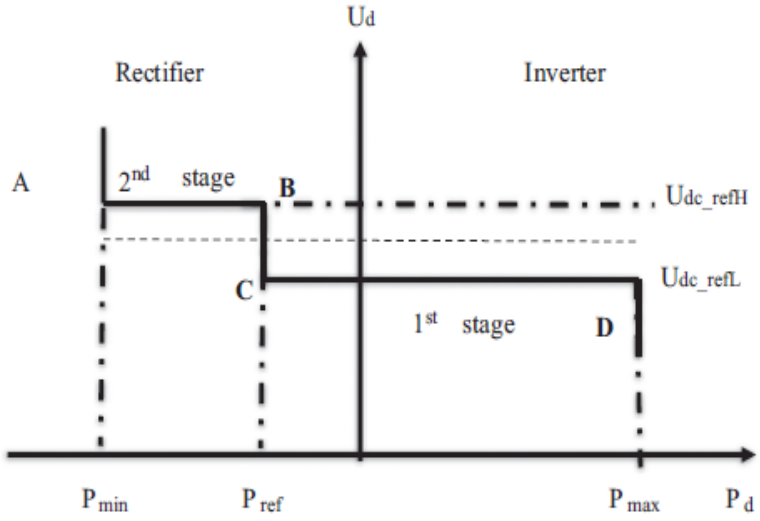
Figure 2. 36: Master-slave dc control.

2.2.1.4.1 (b) Voltage Margin Method

A voltage margin control method is shown in Figure 2.37(a-b) was proposed to overcome the risks of the master-slave control method, such as dependency on fast communication by Nakajima and Irokawa in 1999 [85]. In this method, converters take turns to regulate the voltage depending on the limit of the converter. If the master converter gets saturated (voltage level), the task will be shifted to another converter [86]. The transition between the two references became a major constrain of this method since it causing great stress on the converter such as oscillation of dc voltage, and this may lead to the collapse of the grid [88]. Furthermore, the margin of the voltage must be large enough to avoid interference between the converters [89].



(a)



(b)

Figure 2. 37: Voltage margin control.

2.2.1.4.1 (c) Voltage droop Control

The control of the VSC-HVDC based grid is realized by either a centralized dc voltage control method or droop based dc voltage control, which takes advantage of local voltages and eliminates the need for extensive and fast communication infrastructure as it is required in centralized dc voltage control [90]. The voltage droop control approach is mostly employed in MTDC grids, where several converters take part in regulating the dc voltage. All converters which participate in voltage regulation will share power based on the slope of their voltage droop characteristics [17, 91]. This controlling strategy was first employed in the ac system using power-frequency droop control. When compared to other voltage controlling strategies such as master-slave control

and voltage margin, voltage droop exhibit higher reliability since it doesn't give rise to voltage oscillations [87]. A linear relationship introduced by a droop control scheme includes two electrical variables in the form:

$$y = y^* + k_{droop}(x - x^*) \tag{2.17}$$

When k_{droop} = droop gain

x^* and y^* = set points

x, y = measured variables.

- **Droop Method 1**

Figure 2.38(a) shows the dc droop characteristics between dc current and voltage, and Figure 2.38(b) shows the implementation of dc voltage-d axis current droop control. This application of droop control offers less strict dc voltage regulation, and it facilitates power-sharing between the connected ac grids in a case where two converters are taking part in dc voltage regulation, the first converter can use proportional-integral (PI) controller and the second one can be equipped with droop control. Droop characteristics shown in Figure 2.38(a) can further be explained mathematically by equation (2.18)

$$I_{dc} = K_D(V_{dc} - V_{dc0}) \tag{2.18}$$

Where V_{dc0} is the reference point corresponding to zero dc current, K_D is the constant of dc voltage-current droop. Idc is the dc current and can be approximated in terms of direct d-axis ac voltage V_d and current Id as:

$$I_{dc} = \frac{3}{2}\frac{V_d}{V_{dc}} I_d \tag{2.19}$$

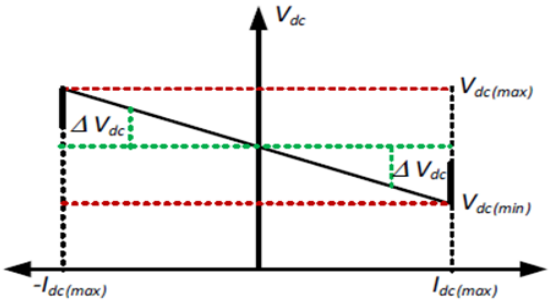
Substituting (5) into (6) will get:

$$I_d = \frac{2}{3} k_D \frac{V_{dc}}{V_d}(V_{dc} - V_{dc0}) = k_T(V_{dc} - V_{dc0}) \tag{2.20}$$

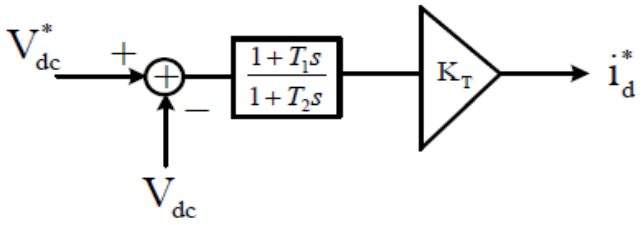
The droop constant is approximated by:

$$k_T = \frac{2}{3} k_D \frac{V_{dc}}{V_d} \tag{2.21}$$

It is based on equation (7).



(a) DC V-I droop characteristic



(b) DC voltage droop control

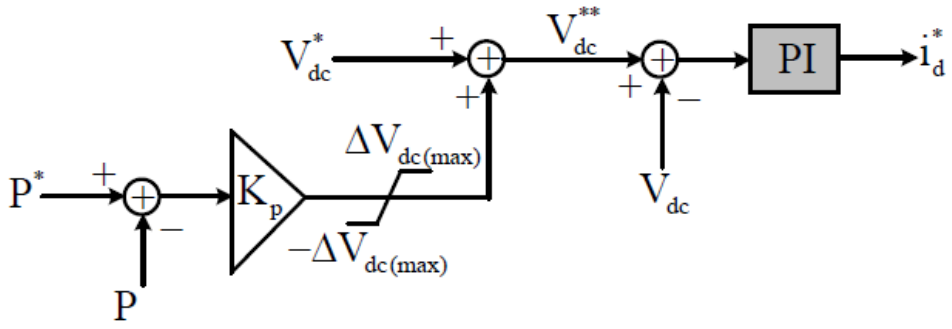
Figure 2. 38: Droop Method 1: (a.) DC V-I droop characteristic; (b) DC voltage droop control.

- **Droop Method 2:**

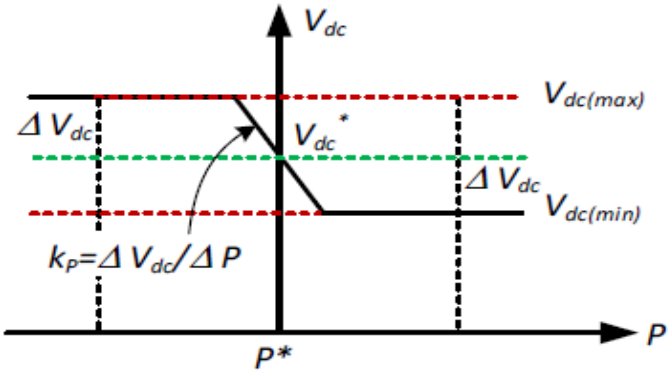
Figure 2.39 (a) shows the implementation of P-V droop control that will allow the conventional dc voltage control to operate with the power control function. This control adjusts the original reference point of the dc voltage V^*_{dc} by a certain amount ΔV_{dc} according to the following expression

$$V^{**}_{dc} = V^*_{dc} + \Delta V_{dc} = V^*_{dc} + k_p\left(P^* - P\right), \qquad (2.22)$$

in order to obtain the set point for power reference P^*. The implemented P-V droop characteristic is shown in Figure 2.39(b), and constant droop Kp is the change in dc voltage over the change in dc power.



(a) V-P_{dc} droop controller



(b)

Figure 2. 39: V-P_{dc} characteristics.

2.3 DC Network: Grid Topologies

The grid topologies are classified into four types, namely: Radial, lightly meshed, densely meshed, and ring structure. The comparison of four types of topologies is in Table 2.3, considering the security, cost, and reliability [92].

Table 2. 3: Distribution network topologies [92]

Topology	**Advantage**	**Disadvantage**
Radial	The structure is simple and has low investment cost	The reliability of this topology is low and has chances to lose a converter in the case of a dc fault.
Lightly meshed	There is a slight increase in security and reliability.	Increase in total line length.
Densely meshed	The reliability is higher, power exchange is more flexible, and the reduction of the shortest connection distance between the two points in the grid.	The cost of this topology is higher, and the length is longer.
Ring	It has simple construction and operation.	This topology is subjected to high losses when they operate in long-distance transmission.

***Radial grid*:** The main characteristic of a radial grid system shown in Figure 2.40 is that power flows in one direction as all the converters are connected to only one dc cable, and there is no need for the bud-bus [93]. It has low reliability and likely to lose a complete converter during the dc-side fault. This topology is a star shape design, and it consists of a series connection that interconnects different nodes [39] [94].

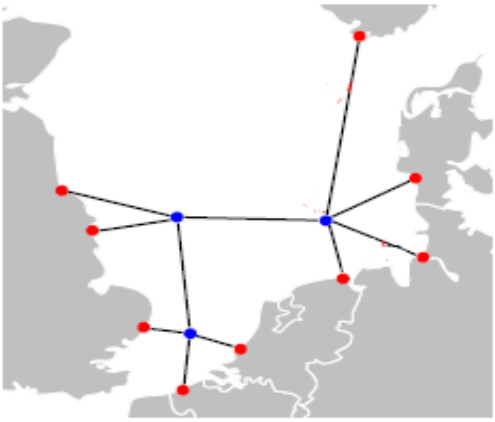


Figure 2. 40: Radial Grid topology.

Lightly Meshed grid: This is recognized as the most reasonable approach due to its flexibility when it comes to power trading, future more its reliability is a bit increased compared to the radial topology. The structure of this topology, illustrated in Figure 2.41 creates an N-1 level of redundancy in transferring power between different zones [93] [94].

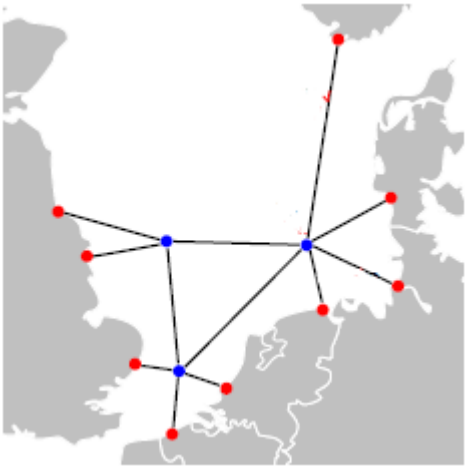


Figure 2. 41: Lightly Meshed grid topology.

***Densely Meshed grid*:** The topology presented in Figure 2.42 is regarded as the most highly flexible among the four topologies, and it the highest level of redundancy since it has the most significant number of connections. Also, the shortest distance between the two points in the grid can be reduced or avoided. However, this topology is expensive when it comes to the cables since they are much longer compared to other topologies [94].

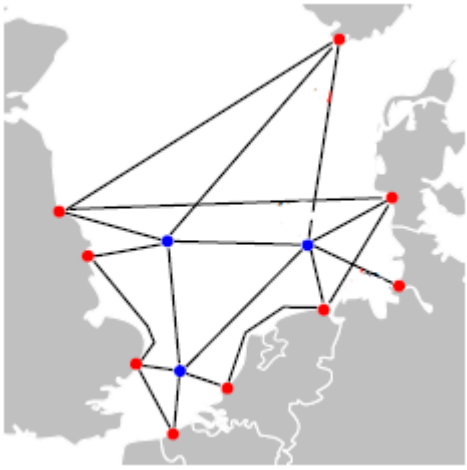


Figure 2. 42: Densely meshed grid.

Ring-shaped grid: All the areas are connected in series, as shown in Figure 2.43, with each other in this topology. The drawback of ring topology it lacks reliability, and it has high losses due to the long transmission distances [94].

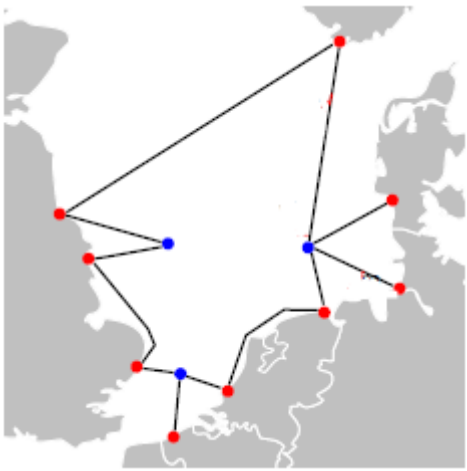


Figure 2. 43: Ring-shaped grid topology.

2.4 Transmission Lines

Reduced Right-of-way (RoW) is one of the key advantages of HVDC over HVAC. In the HVDC network, both dc cables and overhead lines are used in practice. DC cables are mainly restricted by insulator material aging; on the other hand, overhead lines are limited by the annealing temperature of the conductor and thermal expansion (sag). DC cables must be operated at a lesser temperature than bare overhead conductors to ensure the same life expectancy.

2.4.1 HVDC Cables

HVDC connections use three main types of cable: self-contained fluid-filled, extruded, and mass-impregnated. Of these, extruded and mass-impregnated are the most commonly used types. A typical XLPE HVDC cable conductors shown in Figure 2.44 can be buried underground or be laid on the sea bed and. The high voltage cable conductors are covered by proper layers of insulation, water blocking, screening, and mechanical protection that is strong enough to allow underground burial and to operate in the sea [95].

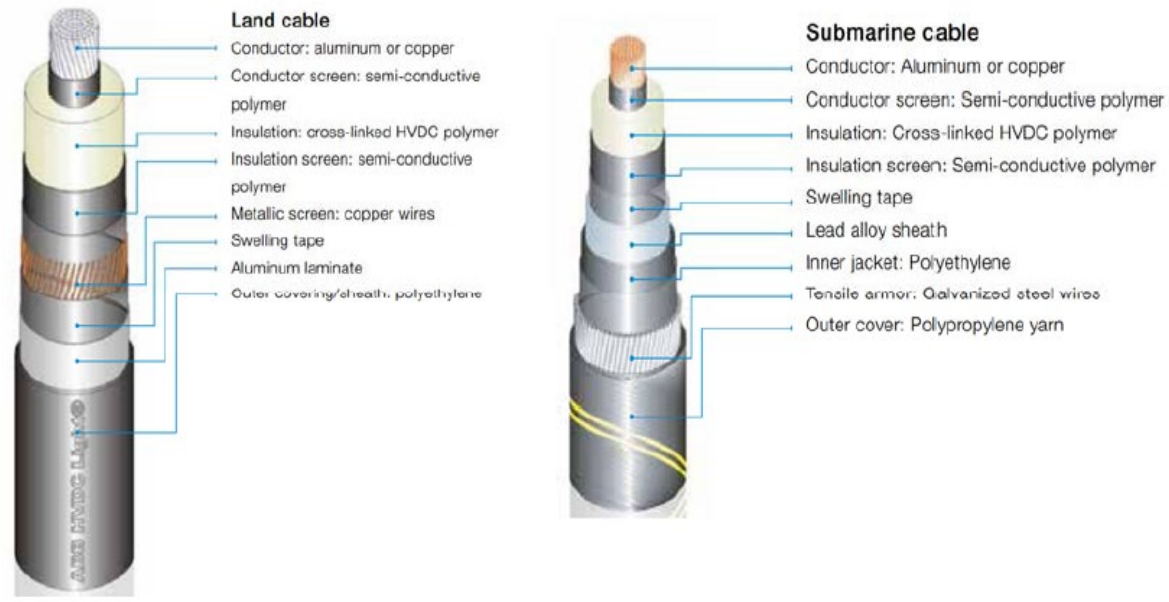


Figure 2. 44: XLPE land and submarine HVDC cable [96].

DC cable advantages are [44] as follows:

- HVDC cables are mainly practical for long-distance underwater bulk energy transmission.
- There is no reactive compensation required at intermediate points as in the case of ac transmission systems, and dc cable lengths are not limited by charging currents.
- DC cables are more economical for the same power rating when compared with ac cables due to conductor and insulation savings.

2.4.2 Overhead Transmission Line

The key components of HVDC overhead lines include RoW, towers, insulators, and conductors. Tower structure requirements for the HVDC line are generally defined by type, material, footing design, number of circuit and configuration, weight loading, and capacity to withstand wind loading. Line insulators provide a means by which power conductors are suspended, and they insulate energized from suspension point [95]. Overhead lines installation cost is low compared to cables in long distances for bulk power. Table 2.4 illustrate typical dimensions and configuration example of existing HVDC transmission lines.

2.4.3 Line Model

There are several possible line models to be used for transient faults in the network. These models are explained in detail in this section.

2.4.3.1 Frequency-Dependent Parameters

A number of existing models for the ac transmission lines can also be used in dc transmission. The best line model takes into consideration the frequency-dependent, distributed parameters, and more than one wave propagation. A frequency-dependent model proposed by A. Budner was one of the first models, but it lacked accuracy due to the oscillatory nature of the solution. The idea of weighting functions was an advanced development that aimed to improve the model. The evaluation of these functions is difficult in time domain since there is a train of peaks due to the continual reflections of the waves at both ends of the line. However, the introduction of change of variables and proposal of single-mode propagation forward traveling (2.23 a and 2.23 b) and

backward traveling functions (2.23 c and 2.23d) improved the weighting function [16].

$$F_r(s) = V_r(s) + Z_0(s).I_r(s) \quad (2.23\ a)$$

$$F_s(s) = V_s(s) + Z_0(s).I_s(s) \quad (2.23\ b)$$

$$B_r(s) = V_r(s) - Z_0(s).I_r(s) \quad (2.23\ c)$$

$$B_s(s) = V_s(s) - Z_0(s).I_s(s) \quad (2.23\ d)$$

Where V_s and I_s are the sending-end values and V_r and I_r receiving-end value $Z_0(s) = \sqrt{(R+sL)/(G+sC)}$ is the line impedance, *F* and *B* are forward and backward traveling function.

2.4.3.2 Frequency Independent Parameters

2.4.3.2 (a) Series Impedance: It's the simplest cable model that involves only a single series impedance and disregards all cable capacitances. This model is suitable for steady-state simulation, and it is not recommended for long HVDC cables.

2.43.2 (b) Cascaded lumped Pi-sections: The model takes cable capacitance into consideration using a certain number of cascaded pi-sections with lumped as shown in figure 2.45, admittances and frequency independent cc whereas the highest frequency that can be represented by the cascaded pi-circuit is estimated by the following equation

$$f_{\max} = \frac{N.c}{\pi.l}, \quad (2.23)$$

Where N = total number of pi-sections,

c = traveling speed of the wave

l = length of the line

In comparison with distributed parameters, lumped parameters are found less accurate except when a simulation time step is more significant than the line traveling time. Also, pi-sections causes an artificial ringing in the waveform due to the reflection at the junctions between two neighboring pi-sections.

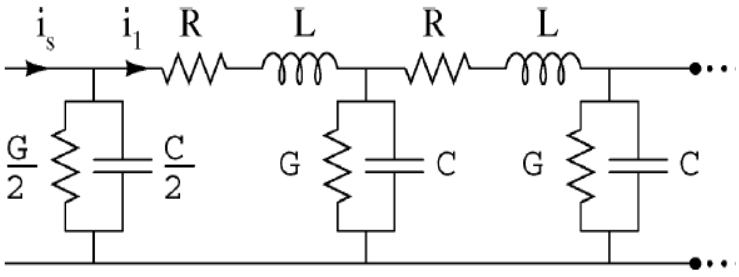


Figure 2. 45: Cascaded lumped pi-sections Transmission line model.

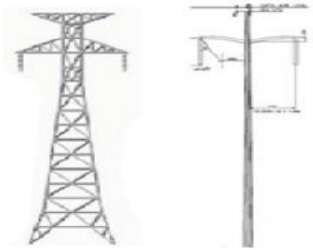
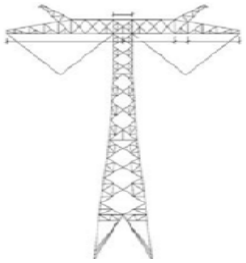
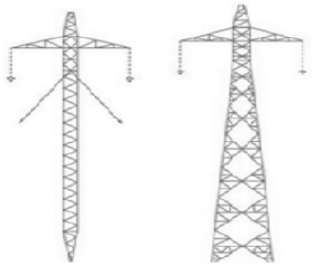
2.4.3.2 (c) Distributed parameters

In cases where lines are frequency independent, distributed elements, a traveling wave theory has to be considered, and line resistance is included ina distributed form. In systems where the fundamental frequency is dominant, the line model with frequency-dependent is regarded as accurate models [16].

2.43.2 (d) Bergeron Model

The distributed nature of the line parameters is of interest in Bergeron's model, excluding line resistance, which is implemented in the lumped form in the middle of the line and at the line end. When the fundamental frequency is considered and is of interest, and the lines are sufficiently long, this model remains acceptable as a single-frequency model. It is likely to achieve reasonable results provided that $\frac{R}{4} << R_0$, where $R_0 = \sqrt{L/C}$ line impedance characteristic [16].

Table 2. 4: Details of existing HVDC transmission lines.

	Nominal HVDC Voltage			
	+/- 400 kV	**+/- 300 kV**	**+/- 800 kV**	**+/- 500 kV**
Typical suspension tower				
Power rating [MW]	1000-2000	600-1000	3000-7500	1500-3000
Configuration	Monopole/Bipole	Monopole/Bipole	Bipole	Monopole/Bipole
Right of way required	45-50	40	85-90	55-70
Range of tower height	36-51	25-40	39-93	31-51
Minimum ground clearance [m] (subjected to local regulations)	10-11	8.5	16	11-13
Insulator length	6.18 (Porcelain) 5.06 (Composite)	4.34 (Pin and Porcelain Cap) 3.60 (Composite)	12.94 (Pin and Cap)	6.00 (Porcelain)
Number of conductors in a bundle per pole	2, 3, 4	2, 3, 4	6, 8	2, 3, 4, 6

2.5 Converter Station Protection

The purpose of short circuit fault removal and protective clearance is to minimize the disturbance to the system operation, hazard to personnel, and minimize the risk of building damage, and, most importantly, the equipment. The protection systems of the power transmission network should be able to select and trigger a fault within its protective zone and discriminate faults that are outside its operating zone. Figure 2.46 shows distinctive protection zones for a typical VSC monopolar converter station, which are marked from 1 to 4. The ac system protection zone is marked by 1, the protection zone for the converter station is marked by 2 and 3 and marked by 4 is the HVDC gird protective zone [97].

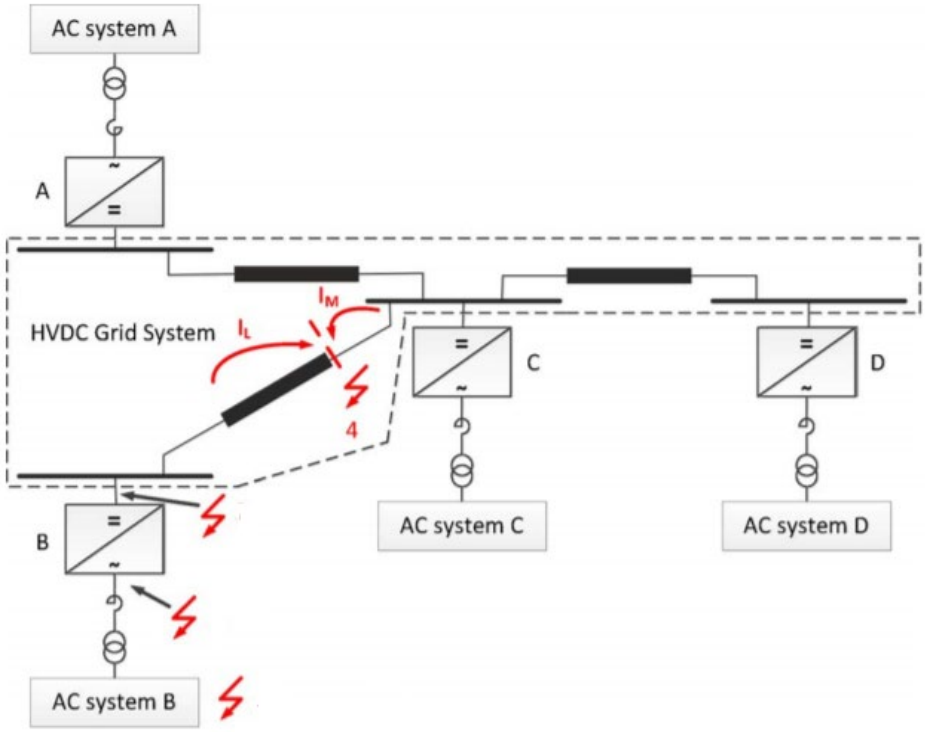


Figure 2. 46: MTDC protection zones.

The ac protective zone (mark 1) includes the following:

- Ac under-frequency and over-frequency protection.
- Ac under-voltage and over-voltage protection ac system faults long duration.

The VSC protective zone (mark 2 and 3), which determine by topology design includes the following:

- Ac under-voltage protection at the converter side (secondary side)
- Valve reactor over-current protection
- Asymmetrical protection at the ac converter aiming to detect a ground fault
- Overcurrent protection for dc-link
- Current differential protection for busbars which will be monitoring and detecting deviations between the sum of converter arm currents and the dc current at the negative and positive dc busbars.
- DC current differential protection detecting ground faults within the circuit up to the converter terminal or dc converter terminals etc.

HVDC grid system protective zone (marked 4) includes the following

- Unbalanced dc line voltage protection which will identify or detect abnormality between positive and negative dc voltages and faults to ground
- Over/under dc voltage protection detecting between negative and positive to ground.

2.6 DC Faults in VSC-HVDC Transmission System.

DC power can be transmitted using either dc cables or dc overhead lines. The choice of transmission is determined by overall optimization considering the capital cost, environmental constraints, and reliability of the transmission system. Usually, the cables are less impacted by the environmental point of view [98]. Any disturbances in the line parameters such as currents and dc voltages on the dc-side as well as currents and voltages on the ac-side affect the power flow in the system. Various faults may occur in the HVDC transmission system, and the disturbances depend on the following [99]:

- Type of faults, such as line-to-ground (L-G) and line-to-line (L-L).
- Earthing scheme provided to dc circuit

Electrical system properties like resistivity, capacity, reactance, and linelength.

- DC filters or concentrated dc capacitors that are present.

- DC voltage polarity (bipolar, asymmetric monopolar, symmetrical monopolar). Additional equipment like overcurrent limiters.
- The fault clearing scheme.
- Converter configuration

2.6.1 DC Faults on MTDC VSC based.

Multiterminal VSC-HVDC transmission technology is favorable compared to conventional HVDC technology due to the fact that it uses a fully controllable switch, which gives an advantage of power flow reversal because it only changes the direction of current in the converter. In MTDC systems, transient fault response can be affected by many factors such as system configuration, converter type, fault type, and protective operations [100]. However, the use of these fully controlled switches is the main drawback when the system is subjected to dc faults [101]. Under dc faults conditions, Insulated gate bipolar transistor valves fail to block fault current because of the anti-parallel diodes; these anti-parallel diodes ensure the four-quadrant operation of the converter. Faults current flows through the anti-parallel diodes and causes great danger to converters. In a multiterminal system, fault detection is very important so that the fault can be isolated, and the health section can be restored. Possible faults which occur on the are as follows [101]:

- Overvoltage
- Overcurrent
- Positive line to Negative line
- The positive line to ground fault
- The negative line to ground fault

Overvoltage

During the line-to-ground fault, capacitors discharge fast to the ground, and currents flow through the ground and back to the healthy line and finally back to the source. Under the bipolar system, this causes an increased voltage of 2p.u. to the un-faulted [98].

Overcurrent

Overcurrent faults are caused by the system being overloaded; overload occurs as the results of a load increasing passing beyond the rating of the converter. It can also be caused by fault on another part of the system.

2.6.2 DC grid protection schemes

DC grids are subjected to faults as every power system, and therefore, the investigation of MTDC grid protection is essential, and it should include high selectivity and strong robustness. The main objectives of dc grid protection are to avoid damage of faults to components, minimize the impact of faults on the grid functioning, and lastly is to ensure safe operation of the system. In that way, negative effects that may be caused by the faults could be minimized [44]. The HVDC system protection scheme should include the protection of dc transmission lines and protection of the converter station. The protection strategies for MTDC grids should be sensitive, selective, robust, and reliable and have high speed [102]. The following properties are critical when developing an MTDC protection scheme [22] [103]:

1) Identification of faulted line correctly, and avoid mal-operate on healthy line.
2) Fast detection due to high fault currents which is insensitive to noise.
3) Fast dc breakers with sufficient breaking capabilities.
4) The protection should be sensitive to disturbances from renewable energy sources and distributed power integrated to the grid.

- **Reliability**: For the protection scheme to be regarded as reliable, it should include security and dependability. Under security, no action should be taken by a protection scheme when it is not necessary to do so. Whereas for dependability, a correction action should be taken by protection against the fault when needed [44].
- **Robustness:** Protection scheme should be able to operate even in worse conditions like degraded situations. Duplication of protection can improve protection robustness [44].

- **Selectivity:** The protection system should be able to differentiate the zones of the system, which are separated by selectivity criteria in the fault detection and only isolate the faulted zone in the system.
- **Sensitivity:** The protection should be sensitive enough to detect the correct fault.
- **Speed:** If the system is equipped with fast/speedy protection, damage in equipment can be avoided, and it should be fast enough to quickly limit the fault current within the maximum interruptible current. Moreover, the disturbance in the network can also be limited or avoided.
- **Stability:** The system should regain its stability operation within an acceptable time after the fault has been cleared [44].

Compared to ac systems protection, dc system protection is difficult due to the following reasons:

1) DC converter terminals need to be protected against any overcurrents as they are very sensitive to overloads.
2) Switching dc currents is more challenging than switching ac.
3) Faulted line identification is enabled through the use of impedance relays in the ac system; however, this strategy cannot be used in the dc system.
4) DC cables are commonly employed in the VSC-HVDC transmission system, which introduces higher steady-state short circuit currents and higher rise times.

The development of a protection scheme for MTDC requires a clear understanding of dc faults and their influencing parameters so that it will be broken down into individual contributions from the faulted feeding network [104].

2.6.3 Fault Detection

The protection against dc faults in the MTDC system remains the major challenge. HVDC circuit breaker protection requires an accurate, fast, and selective relaying algorithm to detect the dc fault in the system. The rapid rise of fault current in the dc grid and low impedance nature of the dc lines/cables are the key challenges for dc fault detection. Various fault detection algorithm

has been proposed, especially methods which are based on only local measurements. Some of these algorithms are summarised briefly [105].

Overcurrent Protection: The operation of this protection scheme is easy, but it lacks selectivity. Generally, when the current exceeds the certain pre-set threshold, the signal will be sent to trip the breaker. One of the requirements of this protection scheme is a high current threshold value; however, this will lead to some delay as the dc breaker will take longer to reach the fully open position. Furthermore, in the occurrence of high impedance fault in the dc system, the fault might not be detected since this will result in high voltage but low fault current, and in cases like these, the fault current might not exceed the threshold value. Overcurrent protection is highly recommended to be used as secondary or backup protection [106].

Current differential protection: This protection is simple and easy to implement the fault protection algorithm; it's commonly used in ac systems protection and provide intrinsic selectivity. But in the dc system, it is not the case; the method has problems of circuit breaker mal-operation caused by cables capacitive current during voltage transients. To avoid long delays in fault detection, fast communication between the converters is essential since the direction of the current at each dc terminal is compared in this technique. Secondly, solving selectivity issues in dc line becomes a challenge due to the long length of the transmission line [106].

Under-voltage protection: Fault detection is done through comparing measured voltage surge, which is caused by the fault with corresponding threshold values. In the ac system, this method plays a significant role, but in the dc system, it is unable to achieve proper discrimination of the fault among the converters during the occurrence of the fault since the voltage across all the converter stations will drop [106]. The drawback of this scheme is low accuracy in selecting a fault; it can work better as secondary protection or back up.

Voltage derivative protection: The occurrence of dc line fault initiates the traveling waves causing the dc voltage and currents to decrease and increase at a rate. This protection scheme uses the traveling wave method, and it's generally used as the main dc transmission line protection scheme. When dc currents and voltages are measured, the derivatives $\partial I / \partial t$ and $\partial V / \partial t$ are

then calculated. The sign of the current derivative is used to indicate whether the fault is located in the dc yard or on the line. This protection works such that it compares the weighted sum of the derivatives given by (2.25) and will be compared to a set threshold. If the calculated derivative exceeds the threshold, the protection will be activated [107]

$$\in = K_1 \partial V / \partial t + K_2 \partial I / \partial t \quad (2.24)$$

Where $\in$ is a weighted derivative sum and K_1 and K_2 are the assigned weights.

Wavelet-based Fault Detection: Protection strategies such as wavelet analysis are regarded as powerful signal processing methods. It is well suited for detecting local changes in a signal and abrupt changes using a time-scale region. Mother wavelet function is used to decompose the signal into different scales and translate it to match an input signal locally. For fault detection, three types of wavelet can be used, namely the discrete wavelet transform, the continuous wavelet transform, and stationary wavelet transform [103]. This protection scheme consists of filter banks, and it doesn't require the design for bandpass filters. However, it is not recommended to work as a stand-alone protection method [108].

Traveling Wave Based protection method

The traveling wave method is widely employed in HVDC system protection. The working principle of this protection scheme simply detects the fault current and voltages impulse generated on the line, which travels from the location of the fault to the far ends of the line based on first and second reflections at the terminals. This strategy solves communication problems, and it can handle low impedance fault detection. Furthermore, it can be used as stand-alone protection and [108].

2.6.4 Fault Isolation

Multi-terminal VSC-HVDC grids protection is one of the main impediments for this network because the most existing VSC converter does not have the capability to block dc fault current. The application of the ac-side circuit breakers is only suitable for the point-to-point HVDC connection as it de-

energizes the entire system; the same approach for HVDC grids protection would not be accepted due to the requirement of HVDC grid to continuously operate the unfaulty lines during the occurrence of the fault. The available technology for the MTDC dc fault isolation circuit breaker is hybrid, mechanical, and solid-state dc circuit breaker [109]. Under dc fault condition, DC CBs are required to selectively isolate a faulty cable/OHL by reliably and quickly breaking high dc fault currents [104]. Fast fault clearing is essentials for DC CBs as it depends on the configuration of the dc transmission system, capacity, series-connected reactors, line impedance, and the voltage source converter topology. The interruption of dc fault current is through forcing the current to zero crossings and the brief discussion on available breaker schemes is given below. Figure 2.47 shows the auxiliary circuit, which is integrated with the dc circuit breaker [110].

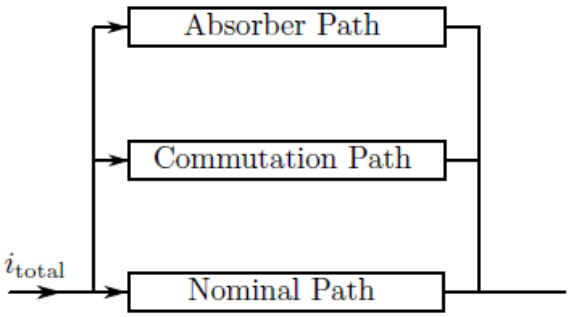


Figure 2. 47: Schematic drawing of an HVDC circuit breaker.

Full Solid State Circuit Breaker

Direct Current Circuit Breakers (DCCBs) such as full solid-state breakers are based on a certain number of GTOs, GCTs, or IGBTs connected in series. Fast reaction times makes these breakers to be an ideal choice for fault isolation. However, on-state losses, especially for IGBTs and the high cost of the components, are their major drawbacks [109]. This hinders the full solid-state breakers from being employed large numbers in the network. This breaker is more suitable for low and medium voltage applications [29] [111].

Hybrid Solid-State CB with mechanical Disconnector

The absence of current zero in dc technologies makes dc current interruption all most impossible. However, auxiliary circuits are developed to help the proposed fault clearing strategies in dc systems by creating current zero. Topologies for hybrid solid-state CBs comprise a current conduction path and current interruption path. To enhance this topology, a small solid-state switch (fast) in series with a fast metal contact disconnector in the main path was proposed as a solution.

Hybrid Mechanical and Solid State CB

This technology includes the combination of the fast performance of a solid-state breaker and the low forward losses of a pure mechanical-breaker in the parallel path. These CBs are faster than common mechanical breakers as only the sufficient voltage must be created by the arc chamber, however no artificial current zero-crossing. If interruption time greater than 20 ms is allowed in the grid or significantly increases the build-up of the arc voltage for commutation, these breakers can be favorable over hybrid solid-state [112]. The design of this hybrid circuit breaker is shown in Figure 2.48, and it is rated at 320kV, 2 kA, and short circuit current breaking capacity rated at 9.0 kA [113].

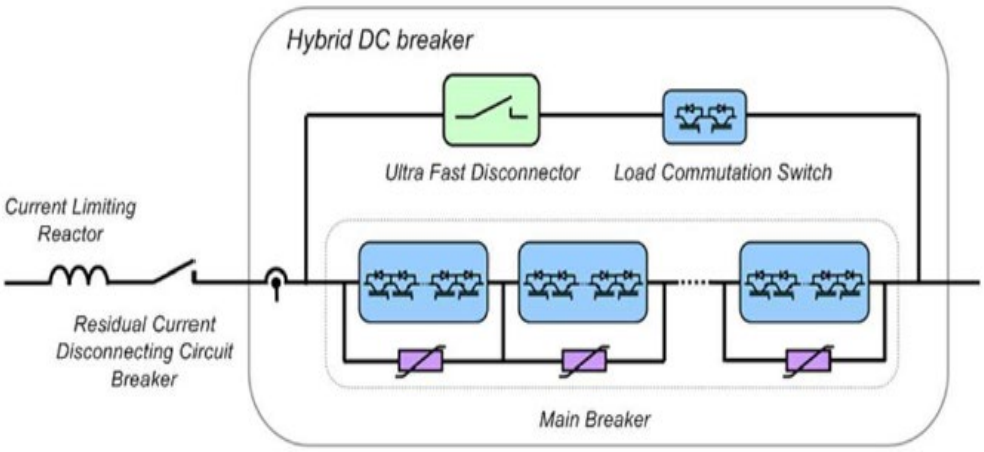


Figure 2. 48: Representation of a hybrid HVDC breaker [113].

A full-bridge based hybrid HVDC circuit breaker is the new type topology that was used for Zhoushan MTDC network, it is rated at 200kV, 2 kA, short circuit current breaking capacity rated at 15 kA, transient voltage 300 kV, power loss

is greater than 0.01% and breaking time of 3ms [23] [114]. Unlike other breakers with low breaking capability, this breaker can deal with severe fault current of a high rise of rate. In the MTDC network, dc circuit breakers are taken as a piece of essential equipment when it comes to grid protection and system stability. DC breakers have drawn a lot of researcher's attention, and the study has achieved significant results [115]. Figure 2.49 shows the topology design of the full-bridge based circuit breaker, which consists of three parallel branches. From three branches, the main branch consists of several full-bridge modules and ultra-fast mechanical to handle the nominal current. In contrast, the transfer branch is made up of several series full-bridge connected with a high switching performance to interrupt the fault current. The absorber branch consists of a surge arrestor to limit the transient interruption voltage. The beauty of this breaker design is the fact that it has negligible state-on losses and it can interrupt the fault current bidirectional. However, a new dc breaker can be developed with stronger current interruptions and less break time [115].

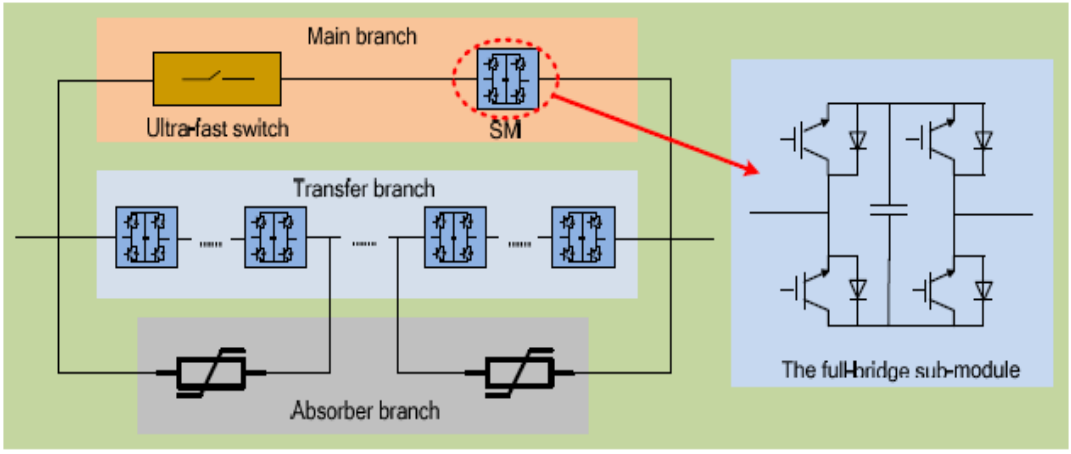


Figure 2. 49: Representation of a Full bridge hybrid HVDC breaker [115].

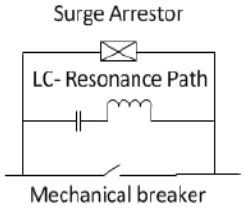
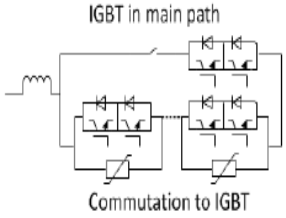
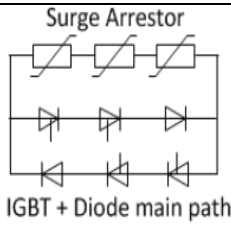
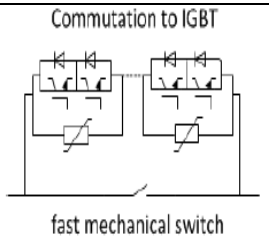
Mechanical Passive / Active Resonance

This technology is based on an ac gas circuit breaker and has been developed for conventional current source converters (CSC) HVDC systems. An additional LC-commutation axillary circuit is connected parallel to the CB. This arrangement enables a current oscillation between the two paths, and it may create an artificial current zero-crossing in the main path in order for the

breaker to interrupt. Passive resonant current zero can be often applied to a metallic return transfer breaker, which normally clears the neutral current in up to a few thousand amperes, which flows through a neutral line of an HVDC transmission system. The passive resonance circuit, which consists of a reactor and capacitor connected parallel across the circuit breaker, this circuit is responsible for generating an expanding current oscillations with a frequency of 1-3 kHz, which ultimately leads to a current zero. Fault interruption takes about 20-40 ms, whereas active resonant current zero is within 8-10ms due to high frequency (several kHz) from the pre-charged capacitor with a reactor and a thyristor switch. The latter scheme can be potentially applicable to interrupt the HVDC fault current where a large capacitor is needed to disrupt the dc current [112] [111].

Table 2.5 contrasts promising circuit breaker innovations in terms of their total interruption period, state losses, and development status.

Table 2. 5: Comparison of HVDC circuit breaker technologies [108]

Typical breaker structure	 **Mechanical Active or Passive resonance CB**	 **Hybrid Solid-State CB with mech. Disconnector**	 **Full Solid State CB**	 **Hybrid Mechanical and solid-state CB**
Max rated voltage	≤550 kV available	120 kV verified by test (up to 320 kV achievable)	≤800 kV (same as voltage level)	AC circuit breakers >500 kV Ultra-Fast-Switches <12 kV
Max rated current	- up to 4 kA proven in operation (up to 8 kA possible with active resonance) - possible to survive transient overcurrents	9 kA experimentally proven (up to 16kA expected)	<5 kA expected	~6-12 kA (estimated)
Expected power loss in comparison to a VSC converter station	<0.001% (metal contacts)	<1% (only few IGBTs in series in the main path)	<30% (large forward voltage due to serial connection of solid state devices)	<0.001% (metal contacts)

Expected total interruption time	<60 ms	<2 ms	<1 ms	<5-30 ms
Required times for commutation and energy absorption	~20ms for contact separation current zero creation ~30ms (passive resonance) ~2ms (active resonance)	<0.2ms for commutation <1ms for disconnector opening ~1ms energy absorption	<0.1ms for commutation ~1ms energy absorption	~20ms for contact separation (conventional AC breakers) ~1-5ms for magnetically driven UFS (Ultra-Fast Switch) with opening speed >20m/s)
The current state of development	- applied in CSC HVDC - also used as MRTB (Metal Return Transfer Breaker)	- working principle proved - type test and interruption test with downscaled breaker passed	- not yet built for HVDC - development of VSC and CSC boosts technology components are alike	- not yet available - slow AC breakers available - UFS not yet available
Further development steps	- optimization of DC arc chamber for passive resonance to achieve a higher current rating and to minimize the time for current zero creation	- field experience with prototype in a test grid - reduction of IGBT costs	- development in solid-state device technology to reduce on-state forward voltage and number of modules in series	- development of ultra-fast-mechanical drives to reduce commutation time

2.7 DC line faults

Short-circuit faults such as line-to-line in Figure 2.50 and line-to-ground in Figure 2.51 are potential sources of transients in the HVDC network. In cable systems, line-to-ground faults are less frequent but are mostly permanent and require repairing the affected cable. The development of line-to-ground faults is caused by the aging of cables main insulation or external damage due to anchoring in the case of sea cables or digging. On the other hand, OHL systems pole-to-ground fault can be the result of lightning strikes or direct touching of the conductor to an external object. After the occurrence of a fault in both OHL and cable lines, the voltage at the location decreases within a few microseconds to the level given by the fault resistance. The magnitude of fault current high depends on the characteristics of the soil like de-ionization and ionization-time constant, soil resistivity, lastly, the tower footing resistance has to be added in the case of a tower back-flash in OHL systems [116] [117]. During pole-to-ground faults, ground fault resistance cannot be ignored as it plays a significant role in the system behavior. The value of ground fault resistance can vary significantly and can be incorporated into the short circuit analysis. Depending on the value of tower footing resistance, voltage stresses across the line insulation can be reduced if the resistance value is low [118] [119]. Analysis of the fault response is thus essential in determining the challenges involved in dc grid protection.

Line-to-ground fault

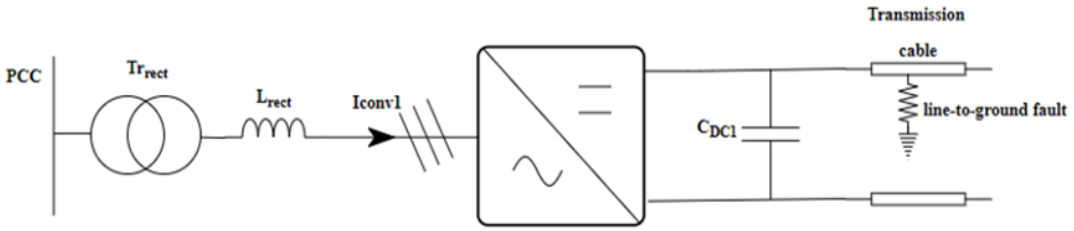


Figure 2. 50: Representation of the Line-to-ground fault.

Line-to-line fault

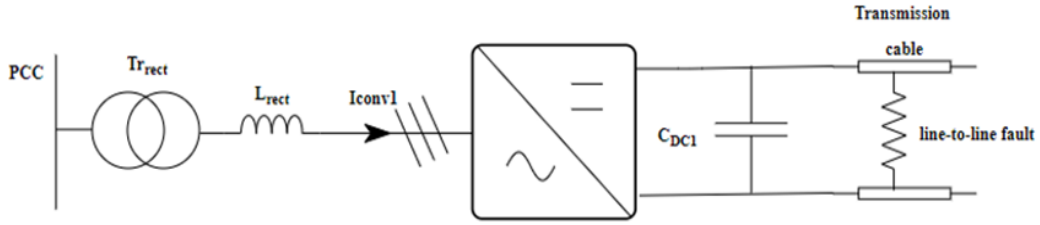


Figure 2. 51: Representation of the Line-to-line fault.

2.7.1 Two-level VSC Cable Pole-to-ground Fault Response

When a positive or negative line is in contact with the ground a fault will occur, and it's called a ground fault, as shown in Figure 2.52. These types of ground faults can be caused by the occurrence of a lightning strike in the overhead lines. This may cause permanent fault when the line break and falls to the ground, and the line must be isolated and repair[120]. The ground fault response depends on the grounding of the system, such as a neutral grounding point on the ac step-up transformer and mid-point grounding on the dc-link [121].

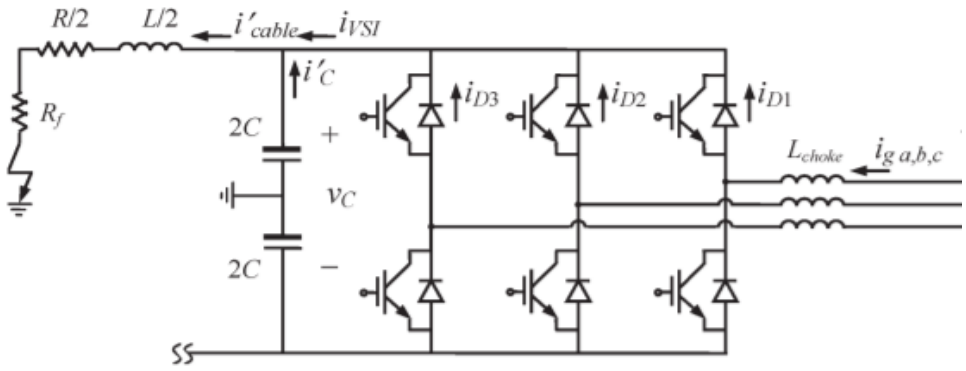


Figure 2. 52: Pole-to-ground fault.

1) (Natural Response) Capacitor Discharge Stage shown in : Unlike pole-to-pole fault where dc-link voltage becomes zero, pole-to-ground faults during the first stage dc-link voltage doesn't drop to zero, so the freewheeling diode stage won't take place. Assuming $R_f + R/2 < 2\sqrt{L/4C}$ the result of the natural response from the second-order circuit gives a non-oscillating discharge

process. The natural response under initial conditions when the fault occurs at *time =0,* $i'_{cable}(t_0) = I_0$ and $V'_c(t_0) = V_0$ are [120]

$$i'_{cable} = 2C\frac{dV'_c}{dt} = A_1\rho_1 e^{\rho_1 t} = A_2\rho_2 e^{\rho_2 t} \quad (2.25)$$

$$V_c = A_1 ei^{\rho_1 t} + qA_2 e^{\rho_2 t} \quad V_c = A_1 ei^{\rho_1 t} + qA_2 e^{\rho_2 t} \quad (2.26)$$

Where, $\rho_{1,2} = -\frac{R_f + R/2}{L} \pm \sqrt{\left(\frac{R_f + R/2}{L}\right)^2 - \frac{1}{LC}}$

$$\mathrm{A}_1 = \frac{1}{\rho_2 - \rho_1}\left(\rho_2 V_0 + \frac{I_0}{2C}\right)$$

$$\mathrm{A}_2 = \frac{1}{\rho_2 - \rho_1}\left(-\rho_1 V_0 + \frac{I_0}{2C}\right)$$

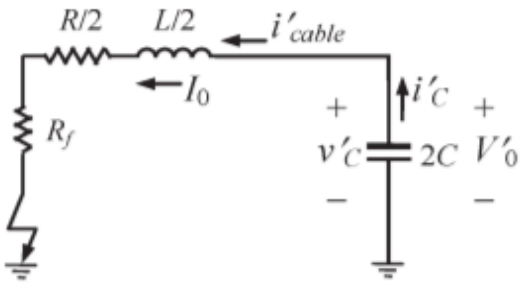


Figure 2. 53: Capacitor Discharge Stage.

2) Grid-side current feeding stage: Figure 2.54 shows the equivalent circuit of the transient phase that can be expressed by the theoretical third-order state-space equation (2.28).

$$\begin{pmatrix} V'_c \\ i'_{cable} \\ i'_{Lchoke} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{2C} & \frac{1}{2C} \\ \frac{1}{L/2} & -\frac{R_f + R/2}{L/2} & 0 \\ -\frac{1}{L_{choke}} & 0 & 0 \end{pmatrix} \begin{pmatrix} V'_c \\ i'_{cable} \\ i'_{Lchoke} \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 1/L_{choke} \end{pmatrix} V_{ga,b,c} \quad (2.27)$$

Where, i'_{cable}, V'_c and i_{Lchoke} are the state-space variables.

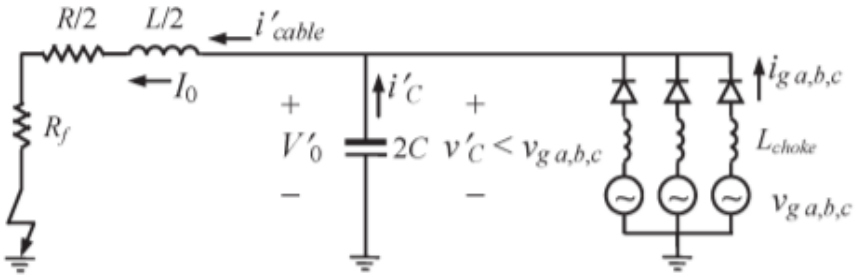


Figure 2. 54: Grid-side current feeding stage [122].

3) Steady State: After the grid-side current feeding stage, the steady-state is reached, and the equation can be determined. The total impedance can be expressed by equation (2.29),

$$Z = \left(R_f = R = j\omega_s L\right) \| \left(1 / j\omega_s C\right) + j\omega_s L_{choke} = | Z | \angle \vartheta^{'} \ , \qquad (2.28)$$

And the current flowing through the diode is

$$iD_1 = i_{ga,}\left(>0\right) = \frac{V_g \angle \alpha}{| Z | \angle \theta^{'}} = \frac{V_g}{| Z |^{'}} \angle \alpha - \theta^{'} \qquad (2.29)$$

2.7.2 Two-level VSC Cable Pole-to-Pole Fault Response

Maturity of ac circuit breakers for ac-side protections makes VSC-based transmission robust under ac fault conditions. On the other hand, dc cable fault remains to be a critical challenge, as shown in Figure 2.55 [123]. Line-to-line faults are less likely to occur, but they can be caused by an object falling across both positive and negative lines on overhead lines. Also, this can be caused by a switching device failing to switch and causing a short. Although this type of fault is less likely to occur, it is more harmful and classified as severe than pole-to-ground and its most critical fault from a protection point of view [102]. The dc cable is assumed to be modeled by a single pi-section where the resistance of the cable is $\left(\frac{R_c}{2}\right)$ and inductance of the cable is $\left(\frac{L_c}{2}\right)$ up to the point of the fault. The capacitance $\left(C_{dc}\right)$ is assumed to be the equivalent capacitance.

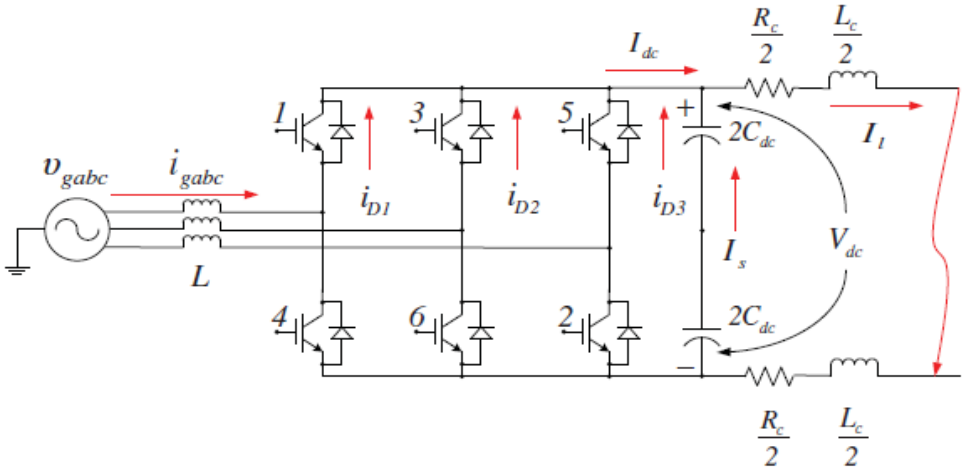


Figure 2. 55: A two-level VSC converter following a line-to-line dc fault [122]

Stage 1. *Capacitor discharge stage (Natural Response)* $(t_0 \le t \le t_1)$: During this crucial stage immediately after the fault occurrence at $(t = t_0)$, the dc-link capacitor starts discharging rapidly [124] shown in Figure 2.56, hence the dc voltage will collapse, and the IGBTs inside the converter station will be blocked [125]. High discharge currents will be generated, but it will decay with time. It is assumed that $R_c < 2\sqrt{\frac{L_c}{C_{dc}}}$ the dc bus voltage and the cable currents expressions are calculated for the R-L-C circuit [120] [126].

$$I_l = C_{dc}\frac{dV_{dc}}{dt} = -\frac{I_0\omega_0}{\omega_n}e^{-\gamma t}\sin(\omega_n t - \xi) + \frac{V_0}{\omega_n L_c}e^{-\gamma t}\sin(\omega_n t) \qquad (2.30)$$

$$V_{dc} = \frac{V_0\omega_0}{\omega_n}e^{-\gamma t}\sin(\omega_n t + \xi) - \frac{I_0}{\omega_n + C_{dc}}e^{-\gamma t}\sin(\omega_n t) \qquad (2.31)$$

Where, $\omega_0 = \sqrt{\gamma^2 + \omega_n^2}$,

$I_l(t_0) = I_0$,

$V_{dc}(t_0) = V_0$

$\gamma = \frac{R_c}{2L_c}$

$$\omega_n = \sqrt{\frac{1}{L_c C_{dc}} - \left(\frac{R_c}{2L_c}\right)^2}$$

$$\xi = \tan^{-1}\left(\frac{\omega_n}{\gamma}\right)$$

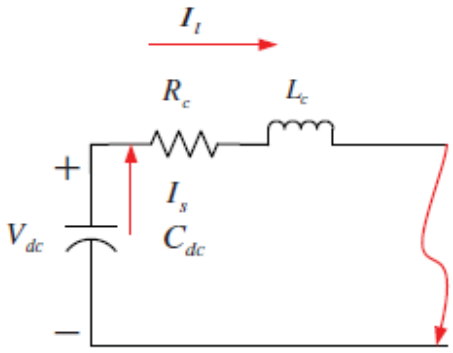


Figure 2. 56: Stage 1. Capacitor discharge stage (Natural Response).

Stage 2. *Diode freewheeling stage (Natural Response)* $(t_1 < t)$: After the discharging of the capacitor $(V_{dc} = 0)$, the dc-link voltage reaches zero, and the ac system is still short-circuited through the free-wheeling diode of the VSC as shown in Figure 2.57. Consequently, the ac system will continue to feed current I_l into the fault even if the converter station is blocked, and the magnitude of these currents are only restricted by the amount of effective impedance between the point of common coupling and the converter terminal. The primary currents of the diodes are high, which may cause the risk of failure to them, but the current decay with time [102] [123] [122] [125].

$$I_l = I_l e^{-\left(\frac{R_c}{L_c}\right)t} \tag{2.32}$$

Where, $iD_i = \frac{I_t}{3}, i = 1,2,3,.....6$

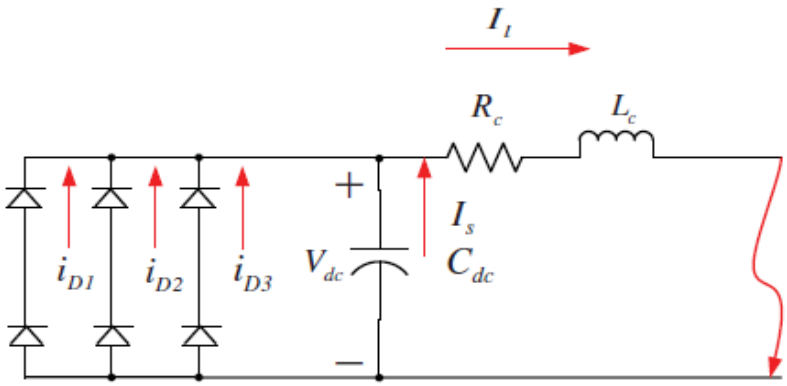


Figure 2. 57: Stage 2. Diode freewheeling stage (Natural Response) [122]

Stage 3. *Grid-side current feeding stage (Forced Response)*: At this stage, cable conductors and dc-link capacitors have a current-source response, where the grid current *(Igrid)* contribution to the dc fault is the sum of the positive three-phase fault currents. Figure 2.58 shows the response determines by the equivalent R-L-C circuit after the IGBTs are blocked due to current rising above the threshold [102] [123].

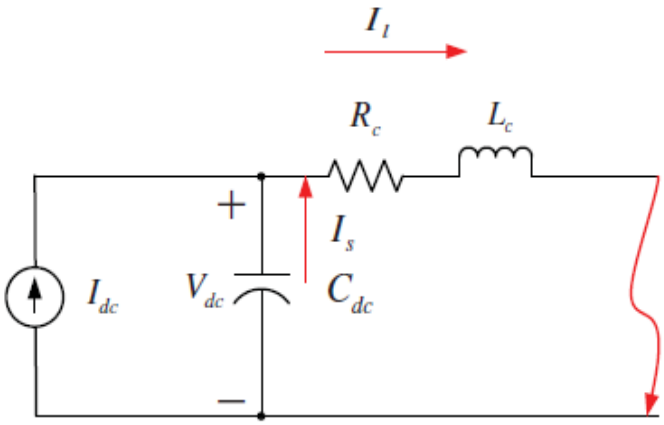


Figure 2. 58: Stage 3. Grid-side current feeding stage (Forced Response) [122]

Stage 4. *AC side Isolation*: The grid current contribution to the fault will be isolated by ac breaker in order to starve the fault. Grid AC isolation won't prevent dc current circulation flowing through freewheeling diodes and ac components such as filter capacitors and inductors, forming an oscillating loop shorted by the diodes [127].

Recharging of the dc-link capacitors

After all the operation of the system during a pole-to-pole fault in a number of stages, the operation continues since the dc terminals are shorted because of freewheeling diodes in the converter. The diode path will now carry both ac and dc fault currents. The current is assumed to be evenly distributed among the three diode branches of the converter, and the diode current is given by [127].

$$\begin{aligned} i_{D1} &= \frac{i_{dc}}{3} + \frac{i_a}{2} & i_{D4} &= \frac{i_{dc}}{3} - \frac{i_a}{2} \\ i_{D3} &= \frac{i_{dc}}{3} + \frac{i_b}{2} & i_{D6} &= \frac{i_{dc}}{3} - \frac{i_b}{2} \\ i_{D5} &= \frac{i_{dc}}{3} + \frac{i_c}{2} & i_{D2} &= \frac{i_{dc}}{3} - \frac{i_c}{2} \end{aligned} \tag{2.33}$$

The anti-parallel diodes in each branch in the converter can rapidly switch on/off phase, depending on the level of fault current in the branch. The fault current distribution has an effect caused by the fast switching of the diode. As given in equation (2.35), the ac phase current will be equal to current for the diodes in the same branch.

$$i_{dc} = i_{D1} + i_{D3} + i_{D5} \tag{2.34}$$

At this stage, the current flowing through the cable is given by

$$i_{cable} = i_{dc} = i_{cables}{}^{*} e^{\left(\frac{R}{L_C}\right)t} \tag{2.35}$$

Where *R, Lc* and i_{cable} are cable resistance and inductance and initial cable current.

Figure 2.59 shows the dc fault characteristic waveform with a sharp rise in cable current. However, even though the cable current rises very sharply during the capacitor discharge phase, the most critical stage for the system is the free-wheeling phase[128]. Therefore, appropriate device protection measures should be considered. When a dc cable fault occurs in an MTDC grid, the converter stations with two-level VSC topology will go through the same stages of response mentioned. Conventional VSC converters cannot

block or control the current during such faults. Since the fault current in the cable rises extremely fast, it is very challenging for the relaying and protection system of such grids.

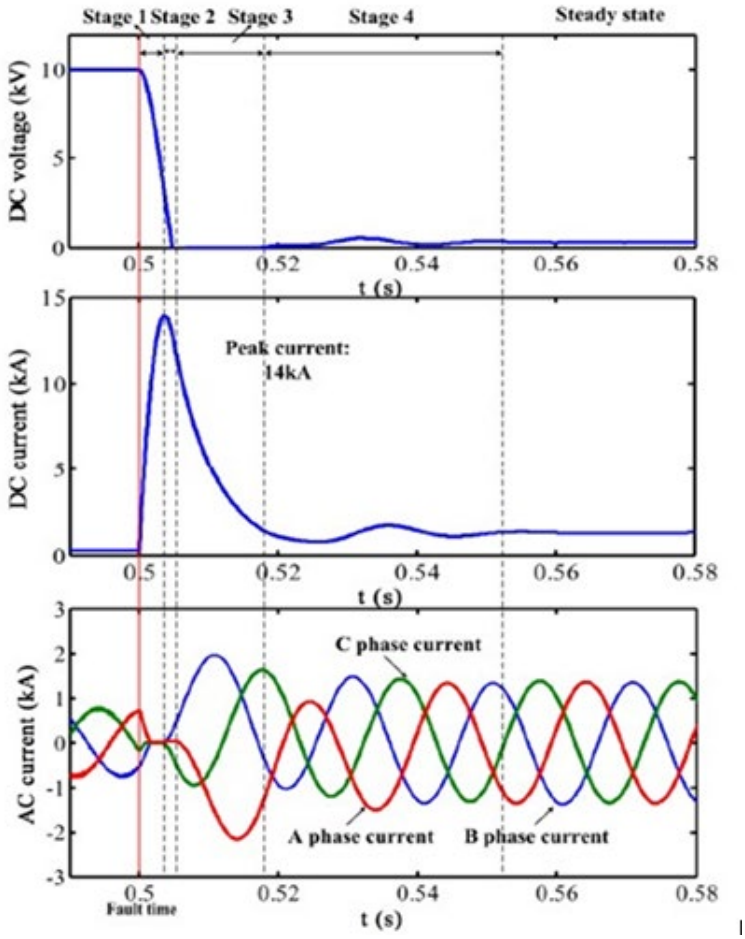


Figure 2. 59: VSC dc cable fault response.

2.7.3 Multilevel (MMC) VSC Cable Pole-to-Pole Fault Response

The half-bridge MMC topology is one of the proposed topologies aiming to improve dc fault in multiterminal and point-to-point HVDC transmission, and it has been widely employed in MTDC systems. Unlike conventional two-level with concentrated capacitors, MMC topology uses distributed cell capacitors, and they do not contribute discharge currents when the converter switches are blocked due to dc fault. Instead, the fault current magnitude of MMC is low. Similar to two-level, half-bridge MMC lacks the ability to block the ac grid currents contribution through freewheeling diode during dc faults [33]. The submodule of the MMC suffers from high fault current and will likely be

damaged; due to this, the entire system will be threatened, especially the grid side [129]. Figure 2.60 shows the half-bridge topology subjected to short circuit (polo-to-pole) fault, and three stages can clearly be distinguished. The stages are classified as Stage 1 with a steep increase of the fault current, stage two it is when the slow and discontinuous decline of fault current is taking place, and lastly, stage three is when the steady-state fault current is maintained, and the fault current is fed only by the ac system [130].

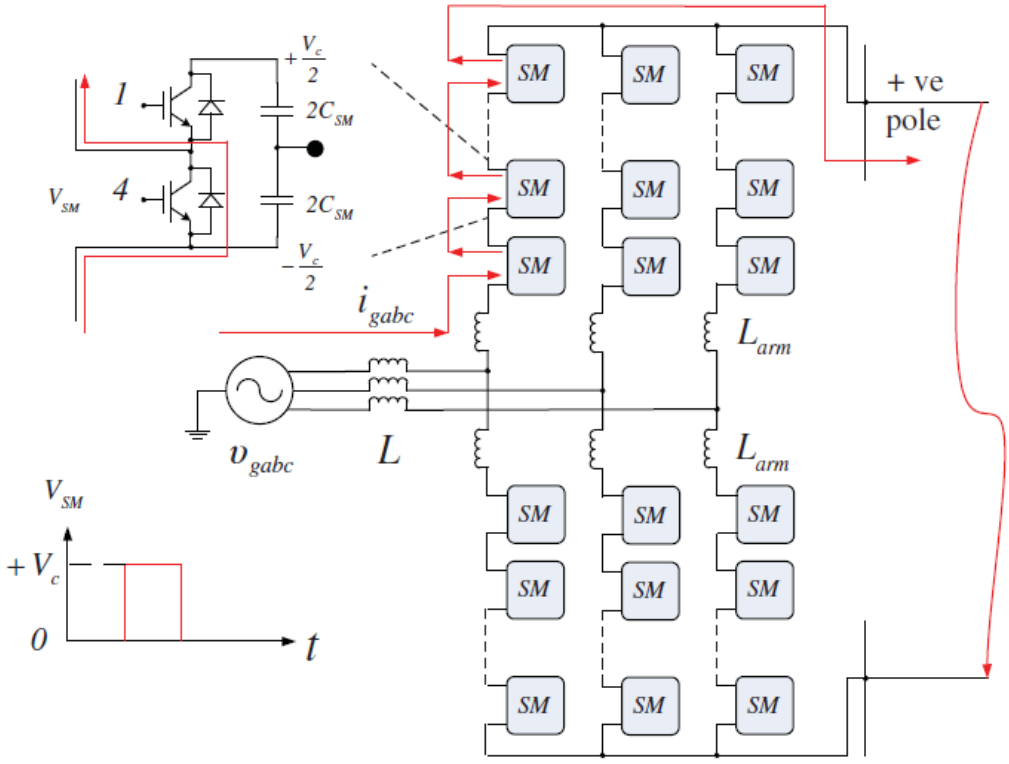


Figure 2. 60: A HB-MMC converter following a line-to-line dc fault.

Stage 1: before IGBTs turn off ($t_0 \le t \le t_1$): It is assumed that all submodules are inserted, and the fault occurs at t_0 and at t_1 the IGBTs are then blocked. At that instance, the ac voltages and currents presented in Figure 2.61 remain unchanged to their respective rated values at the time t_0 [102]. The dc current I_{dc} starts to increase very fast, creating the steep fault current as submodule capacitors discharge through dc side inductance. The lower and upper arm currents are increase and almost identical [130]. It is observed that when the arm current is positive at the moment, the converter is blocked, the submodule

capacitors will continually discharge until the arm current becomes zero. This can cause a small delay between the converter block signal being processed and the initialization of stage two [131]. At the end of the interval the phase-a currents are given as:

$$i_{ap}(t_1) = \frac{i_{ga}(t_0)}{2} + \frac{i_{dc}(t_0)}{3} + \frac{V_{dc}(t_0)}{2L_{arm}}(t_1 - t_0) \tag{2.36}$$

$$i_{al}(t_1) = \frac{i_{ga}(t_0)}{2} + \frac{i_{dc}(t_0)}{3} + \frac{V_{dc}(t_0)}{2L_{arm}}(t_1 - t_0) \tag{2.37}$$

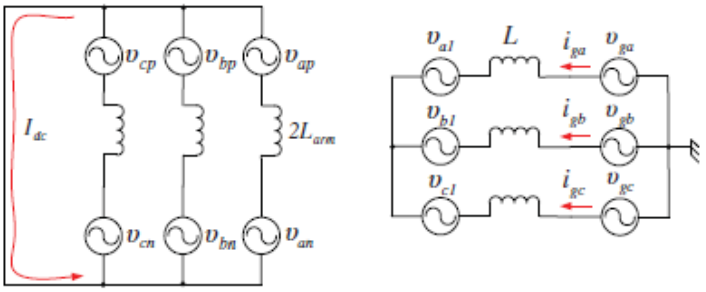


Figure 2. 61: Equivalent circuit of stage 1 response following a line-to-line dc fault.

Stage 2: Diode freewheeling stage ($t_1 \le t \le t_2$): At this stage t_1 , the converter IGBT switches remain blocked and continue. Submodule voltage is prevented from driving the fault current. The contribution from the ac grid starts where the current flows through freewheeling diodes, as shown in Figure 2.62. In this process, each leg of the converter has about the third of the dc line currents flowing in it. All converter arm diodes will be forward biassed, and this results in exposing all three phases in a significant reduction in a load impedance [131]. One converter arm current will increase while the other arm current decreases to zero. The entire ac voltages on the ac grid get applied across the inductor, and that will cause ac currents to increase. The time taken for the current in one arm to reach zero is expressed by

$$t_2 - t_1 = \frac{i_{ga}(t_2) - i_{ga}(t_0)}{L} \tag{2.38}$$

Where $i_{ga}(t_2) = 2\left(\frac{I_{dc}(t_0)}{3} + \frac{V_{dc}}{2Larm}(t_1 - t_0)\right)$

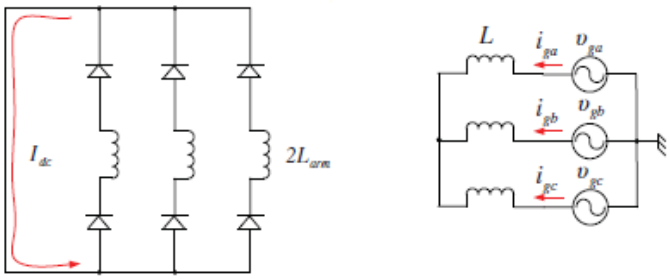


Figure 2. 62: Equivalent circuit of the freewheeling phase response following a line-to-line dc fault.

Stage 3; Grid current feeding ($t_1 < t$):

From Figure 2.63, it is observed that the arm inductor has an influence on the grid current. Since the inductor has a direct impact on the current flowing in the diode, the relationship to design the L_{arm} has formulated to limit the current magnitude to $i_{D\_\max}$ for nominal values of dc bus voltage V_{dc}, IGBT turns off time t_1 and dc current I_{dc} as given in (2.40).

$$L_{arm} > \frac{V_{dc}}{2} \frac{(t_1 - t_0)}{\left(\frac{i_{D\_\max x}}{2} - \frac{I_{dc}}{3}\right)} \tag{2.39}$$

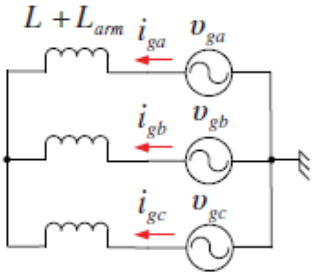


Figure 2. 63: Equivalent circuit of grid current feeding phase response following a line-to-line dc fault.

2.7.4 Earthing Configurations

The design of the earthing system in HVDC is not only designed for fault conditions, but it also includes emergency and normal conditions. Whereas in HVAC systems earthing is only designed for fault conditions. In bipolar topology, an earthing system is used for improving the reliability of the system. In a case where one pole is faulty, the current path will flow through the ground return, permitting the system to operate at about half capacity [95]. Earthing configuration is one of the factors that should be considered when analyzing systems operation. The systems fault current during the line-to-earth fault depends on the formation of current loops generated by the shared earth within the system. There are several earthing configurations that are possible in the converter stations and earthing occurs at a number of possible points, for example:

- DC-link capacitor midpoint
- AC transformer neutral point
- Each cable end

Presently there is no official earthing of MTDC systems that have been not yet defined. However, implantation of various configurations is currently carried out in point-to-point since it's widely used. As for MTDC systems, there is a little practical experience, and this could pose serious challenges to the proposed super-grid, which could possibly integrate converters with varying earthing configurations based on the standards of the local system operator.

It is a common practice to earth the ac transformer on the ac grid side, leaving the converter side to unearth; however, work has been proposed to make practical and effective use of an earthed Y connection on the converter side of the transformer. This practice aims to help limit the high line-to-line dc voltage produced by single-phase to earth fault on the converter side. Moreover, this will allow the positive and negative lines to rebalance after the fault. The system's behavior also depends in the type of earthing used as one of the key factors, listed below are two available options and potential earthing points within the converter are shown in Figure 2.64 [34, 115]:

Low impedance (solid): The healthy line is subjected to double pole-to-earth voltage during the fault.

High impedance: The system can behave like it's unearthed if the value of impedance is high enough. Also, it limits the fault current [39].

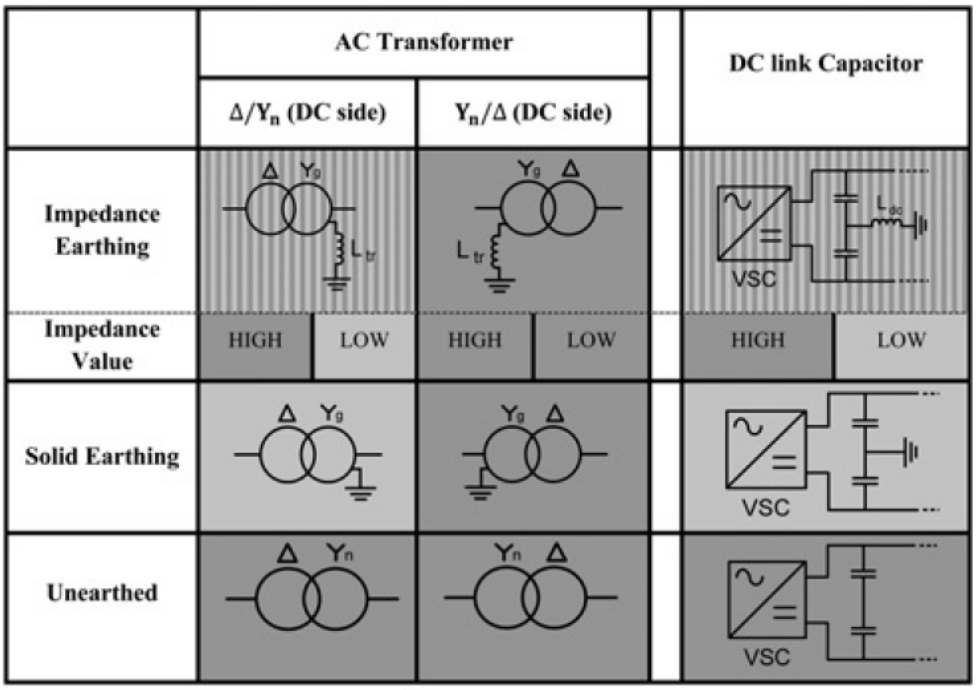


Figure 2. 64: Potential earthing points of dc converter system [34]

CHAPTER 3: VSC-HVDC MATHEMATICAL MODELLING

This chapter presents detailed mathematical modelling of a two-level VSC topology emphasizing on basic operating principle, ac-side, and dc-side dynamics. VSCs can be represented by several established modelling approaches in electromechanical and electromagnetic transient studies. In this research, a detailed switching model approach.

3.1 Basic Operating principle of a 2-level VSC Converter

Figure 3.1 shows one phase of a two-level VSC-HVDC converter

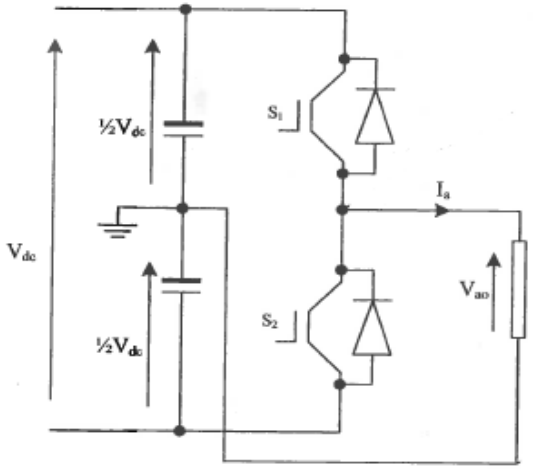


Figure 3. 1: One phase of a two-level converter.

A two-level converter has two switches per phase, as shown in Figure 3.1, and it generates two voltage levels: ½ Vdc and -1/2 Vdc. In a two-level VSC topology, switches are working in a complementary manner and are paired (S_{a1}, S_{a2}), (S_{b1}, S_{b2}) and (S_{c1} and S_{c2}). The pair can be described by: S_{a1}+ S_{a2} =1, S_{b1}+S_{b2}=1 and S_{c1}+S_{c2}=1. When the upper switch is on (S_{a1} =1), the lower switch should be off (S_{a2} =0), and the same pattern applies to phase b and c. Based on this, the converter terminal voltages *a, b,* and *c* relative to the midpoint *0* can be generated from the dc-link voltage V_{dc} as given by equation (3.1) [62].

$$V_{a0} = \frac{1}{2} V_{dc}(S_{a1} - S_{a2})$$
$$V_{b0} = \frac{1}{2} V_{dc}(S_{b1} - S_{b2}) \quad (3.1)$$
$$V_{c0} = \frac{1}{2} V_{dc}(S_{c1} - S_{c2})$$

Equation (3.1) basically shows that switching S_{a1} on connects the converters output phase *a* to *½* V_{dc}

And turning S_{a2} on while S_{a1} is off, it's connect S_{a2} output phase "a" to *-1/2* V_{dc}.

3.2 2-Level Converter AC side dynamics

The transients on the ac side are described by equation (3.2):

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \frac{V_{a0} - V_{ag}}{L_i} \\ \frac{V_{b0} - V_{bg}}{L_i} \\ \frac{V_{c0} - V_{cg}}{L_i} \end{bmatrix} - \begin{bmatrix} \frac{R_t}{L_i} & 0 & 0 \\ 0 & \frac{R_t}{L_i} & 0 \\ 0 & 0 & \frac{R_t}{L_i} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (3.2)$$

Where R_t = Resistance of the interfacing reactor

L_t = inductance of the interfacing reactor

V_{a0}, V_{b0}, V_{c0} = Converters output voltages

V_{ag}, V_{bg}, V_{cg} = Grid voltages

The basic equations describing the system behavior are expressed using Kirchhoff's voltage law. The ac grid voltage is defined as E_{abc} and ac currents defined as I_{abc} , resistance, and inductance between the converter and the grid is defined as *R* and *L*, and converter voltage is V_{abc} as seen in Figure 3.2. The grid voltage side of the converter can be described as:

$$E_{abc} = Ri_{abc} + L\frac{d}{dt} i_{abc} + V_{abc,conv} \quad (3.3)$$

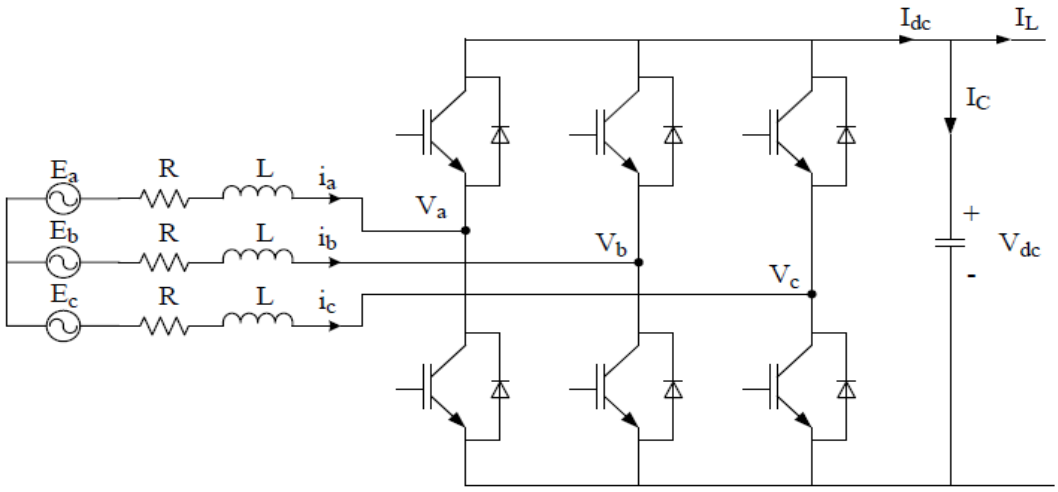


Figure 3. 2: Schematic representation of the VSC-HVDC system.

The three-phase converter voltages and currents are expressed in a 2-axis d-q reference frame using the a-b-c to d-q transformation, rotating synchronously at given ac frequency, ω [42] [132].

$$\begin{bmatrix} E_d \\ E_q \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + R\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{3.4}$$

The transformation of voltage equations in the d-q synchronous reference frame is [133],

$$E_d = L\frac{d}{dt}i_d - \omega L i_q + V_d + Ri_d \tag{3.5}$$

$$E_q = L\frac{d}{dt}i_q - \omega L i_d + V_q + Ri_q \tag{3.6}$$

3.3 D-Q reference frame

From equation (3.4), the equivalent circuit of the VSC in the synchronized d-q reference frame can be seen in Figure 3.3, where the d-axis is aligned with phase-a of a voltage phasor at point X in a abc reference frame and q-axis=0 [56].

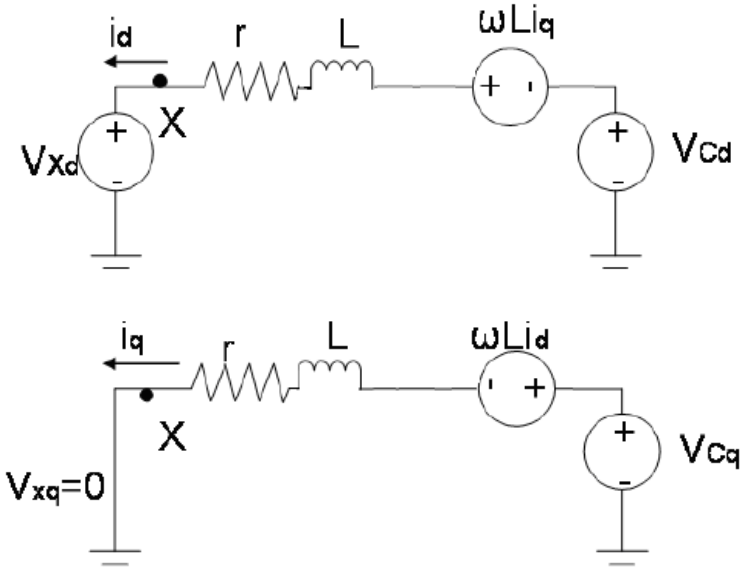


Figure 3. 3: Equivalent circuit diagram of VSC in the synchronous d-q reference frame

From equation (3.5) and (3.6), it can be seen that the *d* and *q* axes are coupled due to the terms ωLi_d and ωLi_q. A decoupled controller, which consist of the PI and feedback loop as expressed in equation 2.14 and 2.15 can be used to solve this problem.

The power in the reference frame is given by [134]:

$$P_{dq} = \frac{3}{2}(V_d i_d + V_q i_q) \tag{3.7}$$

The grid voltage vectors V_d is assigned along the d-axis direction, and then vector V_q (virtual grid flux) is assigned to be acting along the q-axis. With V_q=0, the instantaneous reactive and active power absorbed or injected from the ac system is given by [135]:

$$P = \frac{3}{2}.V_d.i_d \tag{3.8}$$

$$q = -\frac{3}{2}.V_d.i_q \tag{3.9}$$

The relationship between ac side input and dc side output is given as

$$P_{dq}d = P_{dc} = V_{dc}I_{dc} \tag{3.10}$$

Where V_{dc} = dc output voltage

I_{dc} = dc current.

The current in the two-level converter switches can be linked to output phase currents i_a, i_b and i_c by using the switching function given by the equation:

$$i_{Sa1} = S_{a1} i_a \ , \ i_{Sa2} = S_{a2} i_a$$

$$i_{Sb1} = S_{b1} i_b \ , \ i_{Sb2} = S_{b2} i_b \tag{3.11}$$

$$i_{Sc1} = S_{c1} i_c \ , \ i_{Sc2} = S_{c2} i_c$$

The output phase currents can be related to dc-link current I_i by:

$$I_i = S_{a1} i_a + S_{b1} i_b + S_{c1} i_c \tag{3.12}$$

Or

$$I_i = S_{a2} i_a + S_{b2} i_b + S_{c2} i_c \tag{3.13}$$

3.4 DC side dynamics of a 2-level VSC

Considering the dc link concentrated capacitors nodes, the dc-side dynamics of a two-level converter are described as:

$$I_c = I_{dc} - I_i \tag{3.14}$$

$$\frac{dV_{dc}}{dt} = \frac{I_{dc} - I_i}{C} \tag{3.15}$$

$$\frac{dV_{dc}}{dt} = \frac{I_{dc} - \left[S_{a2} i_a + S_{b2} i_b + S_{c2} i_c \right]}{C} \tag{3.16}$$

CHAPTER 4: DEVELOPMENT OF MTDC VSC-HVDC MODEL

This chapter presents the design specifications that are to be used in this study and the implementation of decoupled control loops such as the outer loop and inner loop control of VSCs in PSCAD software.

4.1 Two-level VSC HVDC system model

A 4-terminal radial VSC-HVDC test model parameters are given in Table 4.1 is modelled in PSCAD, and it can work either as rectifier or inverter depending on the demand. The test model is designed to be radially mashed MTDC, configured to be a symmetrical monopolar based in 2-level VSC converter topology.

Table 4. 1: MTDC Network parameters.

2-LEVEL, SYMMETRICAL MONOPOLE VSC-HVDC SYSTEM SPECIFICATIONS				
	VSC 1	VSC 2	VSC 3	VSC 4
Grid Voltage	420.0 kV	420.0 kV	500 kV	420 kV
AC frequency	60 Hz	50 Hz	50 Hz	60 Hz
DC voltage	400 kV	400 kV	400 kV	400 kV
Active power (P)	0	200 MW	200 MW	0
Transformer ratings	Star/star connection Vprim=420.0 Vsec = 230 kV S= 1500 MVA	Star/star connection Vprim=420.0 Vsec = 230 kV S=1500 MVA	Star/star connection Vprim=500.0 Vsec = 230 kV S=1500 MVA	Star/star connection Vprim=420.0 Vsec = 230 kV S=1500 MVA
System AC filters	q = 25 $Freq_{base}$ = 60 Hz Q = 5 MVar	q = 25 $Freq_{base}$ = 50 Hz Q = 5 MVar	q = 25 $Freq_{base}$ = 50 Hz Q = 5 MVar	q = 25 $Freq_{base}$ = 60 Hz Q = 5 MVar
DC capacitance	C= 300 μF	C= 300 μF	C= 300μF	C= 300μF
System phase reactors	R = 0.015 Ω = 0.005 pu L = 0.002 H = 0.26 pu	R = 0.015 Ω = 0.005 pu L = 0.002 H = 0.26 pu	R = 0.015 Ω = 0.005 pu L = 0.002 H = 0.26 pu	R=0.015Ω= 0.005 pu L = 0.002 H = 0.26 pu

Figure 4.1 shows a single line diagram of the VSC system model; the converter terminal is illustated in Figure 4.2. The system is connected and transmitting power through the use of dc cables. The cable specifications for both positive and negative cables are the same. The system is connected, as shown in Figure 4.2, where six IGBTs are connected, forming a converter with concentrated midpoint-grounded dc capacitors. The converter is connected to the ac grid through a phase reactor and a transformer. The ac side of the system is assumed to be a stiff grid and is modelled as an ideal ac source. The converter terminals are labeled as VSC 1, VSC 2, VSC 3, and VSC 4. The ac side is supplied by 500 kV and 420 kV, whereas the dc grid is maintained at 400 kV dc. The ac circuit breakers are connected to isolate ac faults, but ac faults are not covered in this work as ac circuit breakers are regarded as mature protection scheme.

During normal operation, the system converter is supposed to demonstrate the features of IGBTs with anti-parallel diodes, which is to transmit the power directional. Convertes are controlled such that the total converter current should not exceed the rated current ($I_{max}=I_{rated}$). As an MTDC system, at least two or more terminals should have excess to regulate the dc voltage to avoid instability in the grid during dc faults. As shown in Figure 4.1, VSC1 and VSC 4 are assigned to regulate dc voltage and VSC2, and VSC3 is assigned to control the power.

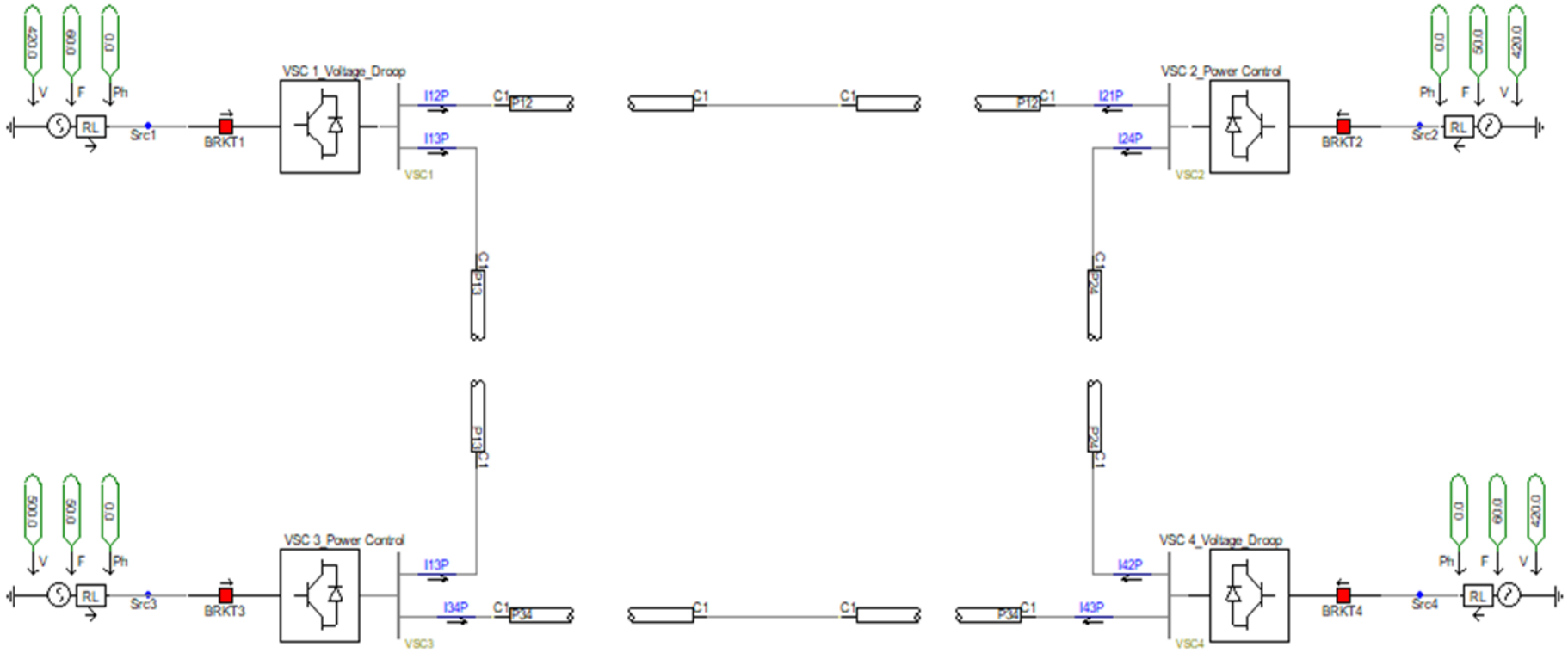


Figure 4. 1: Complete structure of a proposed VSC-MTDC network.

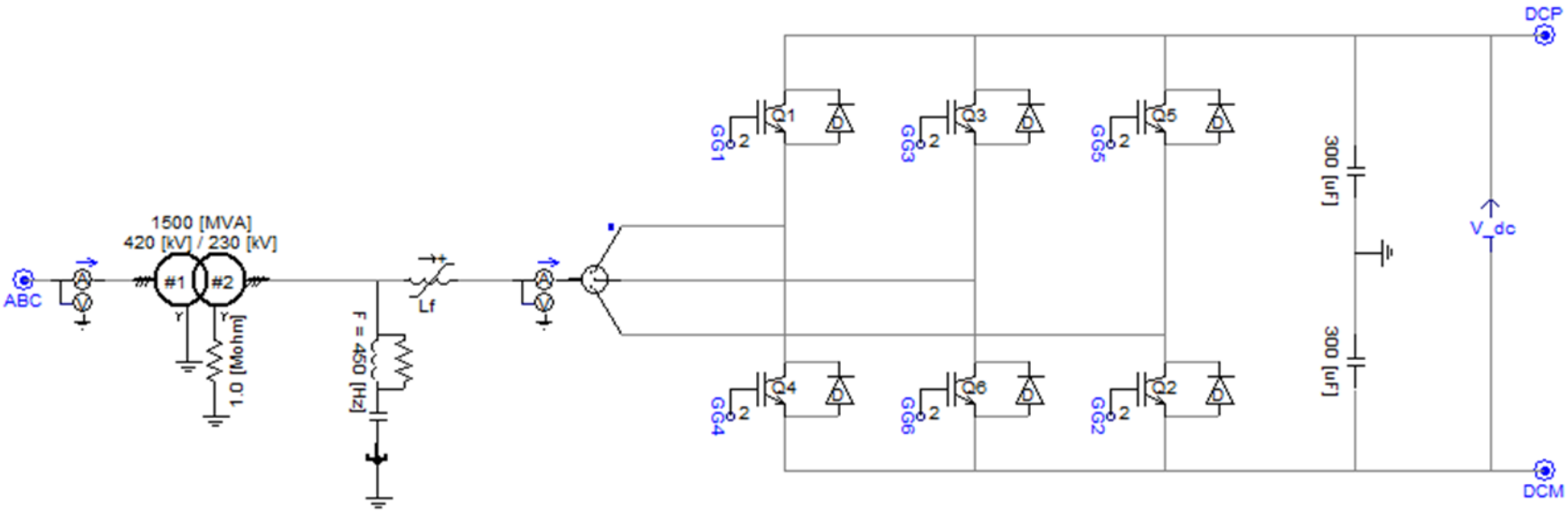


Figure 4. 2: Rectifier-side of a two-level VSC-HVDC based on PSCAD.

4.2 DC Transmission Cable Model

The PSCAD cable model is used in the simulation throughout this work. A real cross-linked polyethylene (XLPE) VSC-HVDC submarine cable rated at 320 kV, was used to design a cross-section of the cable rated at 400kV respecting the diameter of the copper conductor while keeping other properties similar. The cross-section dimensions of all the cable-layers are illustrated in Figure 4.3. A detailed Frequency-dependent (phase) cable model is chosen for this work as it is acknowledged as the most advanced time-domain offered so far, it's a built-in model from PSCAD software. It is the best accurate model for all transmission configurations, and unbalanced cable geometry is included [136]. These cables are set to be 100 km long.

The parameters of the cables in PSCAD/EMTDC are calculated based on the material property of the cable chosen by the user and the geometry. However, the real cable geometry representation is different from that used in PSCAD because the latter doesn't take consider the presence of a semiconducting screen that is present in the actual cable. Furthermore, the core conductor is assumed to be a homogeneous solid conductor, whereas the real cable core conductor is made up of many strands [137].

Table 4. 2: DC cables properties (320 kV XLPE)

Layer	**Material**	**Outer Radius**	**Resistivity**	**Relative Permittivity**	**Relative Permeability**
Core	Copper	0.025125	1.68e-8[ohm*m]	-	1
Insulation 1	XLPE	0.045125	-	4.1	1
Sheath	Lead	0.047125	2.2 e-7[ohm*m]	-	1
Insulation 2	XLPE	0.050225	-	2.3	1

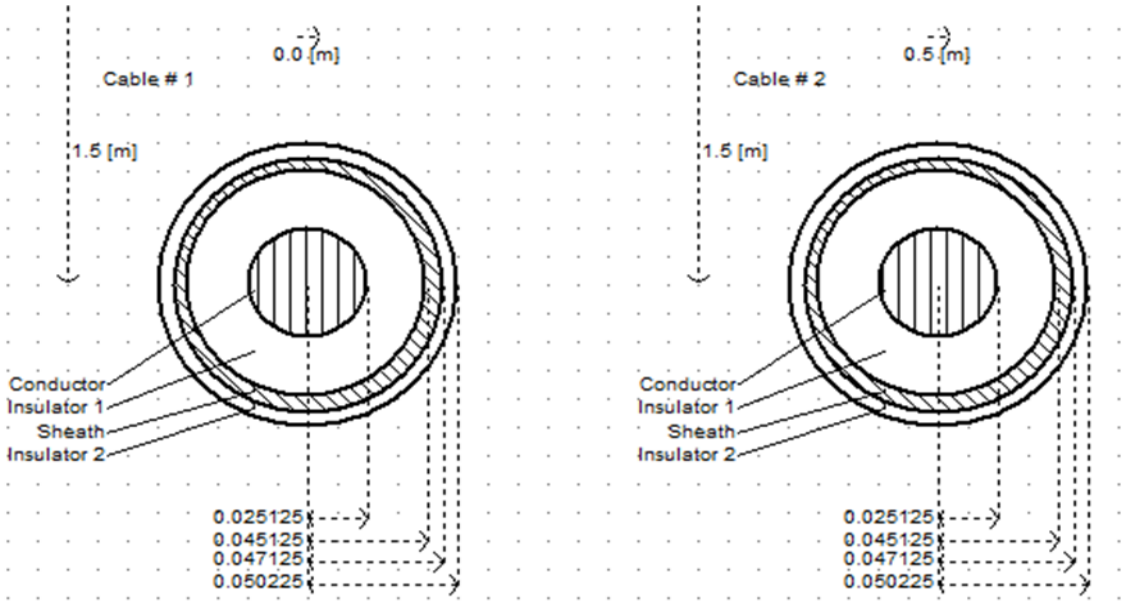


Figure 4. 3: Cable representation on PSCAD.

As shown in Figure 4.3, geometric parameters for the core, sheath and insulation are required on PSCAD.

XLPE HVDC cables shown in Figure 4.4 have shown significant development in recent years. Compared to other HVDC cables, XLPE HVDC cables are:

- Free of oil leaks and are regarded as environmentally friendly.
- Have a faster manufacturing process (homogeneous extruded insulation system).
- Light weight and small bending radius (Easy to install and transportation).
- Have a homogenous extruded insulation system (Possibility of dynamic moving installations).

ABB is one of the XLPE HVDC cable manufactures and they released a new XLPE HVDC cable with a voltage rating of 525 kV and a current rating of 2,5 kA.

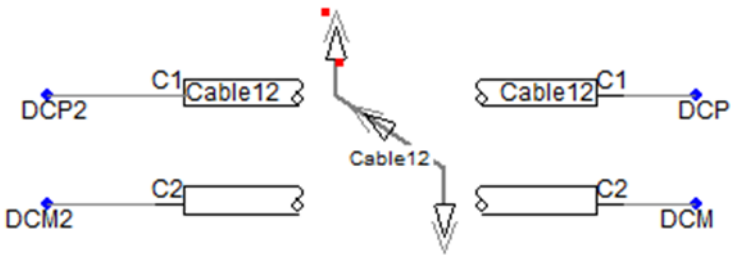


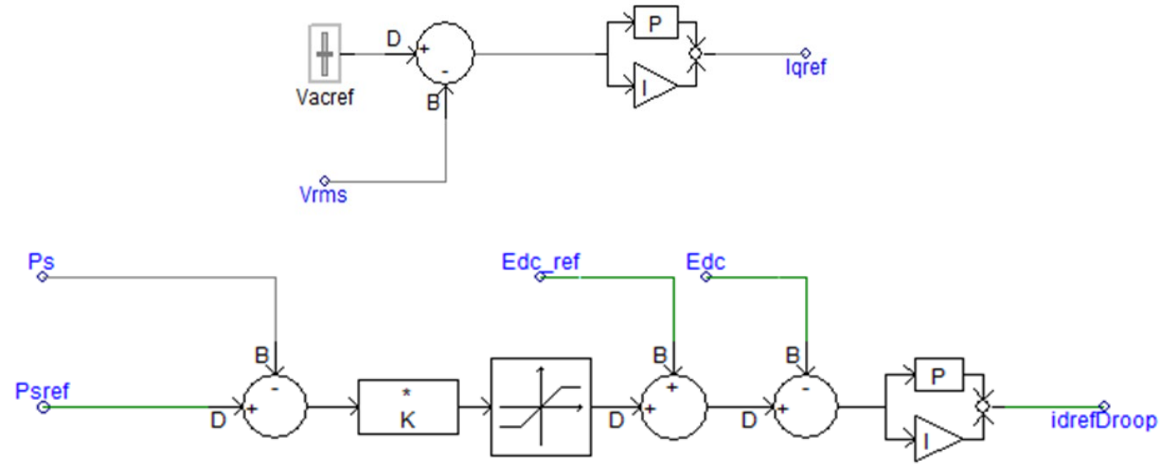
Figure 4. 4: DC cable connection in PSCAD software.

The design of this work includes frequency-dependent model configuration, as shown in Figure 4.3, and the cables are placed 0.5m apart and are at a depth 1.5 m below ground.

4.3 VSC-HVDC Control

4.3.1 Outer Loop Controller

VSC 1 and VSC 4 are designed to regulate the dc voltage and constant reactive power control of 40MVar. Figure 4.5 represents the converter's outer loops controller, which is used to generate d-q components of the inner loop. Figure 4.5 (b) illustrates the dc voltage droop control diagram.

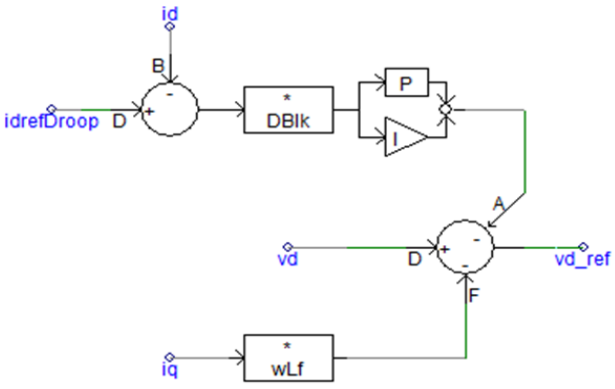


(b)

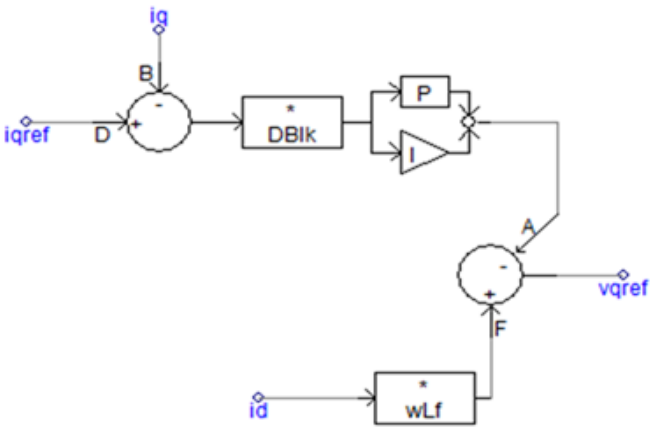
Figure 4. 5: Outer loop implemented in PSCAD software.

4.3.2 Inner Loop Controller

The inner control structure in PSCAD is shown in Figure 4.6 (a-b), where d-q components from the outer controller are used as input.



(a)



(b)

Figure 4. 6: Inner loop implemented in PSCAD software.

Where I_d = d-frame measured current

I_q = d-frame measured current

V_d = d-frame measured voltage

V_q = d-frame measured voltage

ωLf = angular frequency with phase reactance

V_{dref} = d-frame reference voltage

V_{qref} = d-frame reference voltage

The controller gain and time constant parameters must be carefully selected for adequate dc voltage regulation, well-established system stability, and fast response of inner current control. Tuning of the Proportional integral (PI) controller in [138] by optimum modulus method is used for current controller parameters for fast response and simplicity. Proportional gain and time integral are given by equation (4.1) and (4.2) [138] [139] [27].

$$T_{i(pu)} = \tau_{(pu)} = \frac{L_{pu}}{\omega_b \times R_{pu}} \tag{4.1}$$

$$K_{pu} = \frac{\tau_{pu} \times R_{pu}}{2T_a} \tag{4.2}$$

$$K_i = \frac{K_{pu}}{T_i} \tag{4.3}$$

Where, $R_{pu} = R\left(\frac{I_b}{V_b}\right)$ = per unit resistance.

$L_{pu} = \omega_b \times L\left(\frac{I_b}{V_b}\right)$ = per unit inductance.

$T_a = \frac{1}{2 \times F_{sw}}$

K_{pu} = proportional gain

T_i = Time integral constant

Several modulation strategies are discussed in the literature review, and SPWM is used in the test model. Three-phase voltages waveforms are compared with carrier waveform. The linear modulation index which is ranged ($0 < m \leq 1$) is related to ac voltage fundamental components and dc-link voltage using (4.4)

$$v(t) = \frac{m \times V_{dc}}{2} \sin(\omega t + \delta) \tag{4.4}$$

Where m and δ can be calculated as follows:

$$m = \frac{\sqrt[2]{V_d^{\,2} + V_q^{\,2}}}{V_{dc}} \text{ And } \delta = \tan^{-1}\left[\frac{V_q^{\,2}}{V_d^{\,2}}\right]$$

Converters output Line voltage can be expressed by (4.5):

$$V_{abc} = \frac{m \times V_{dc}}{2} \approx 0.5m \times V_{dc} \tag{4.5}$$

Converter switches are turned on and off by gating pulses generated from the PWM block. Figure 4.7 shows how gating pulses are created in order to switch the IGBT's. In the figure, frequency triangular carriers waveform is compared with the fundamental waveform.

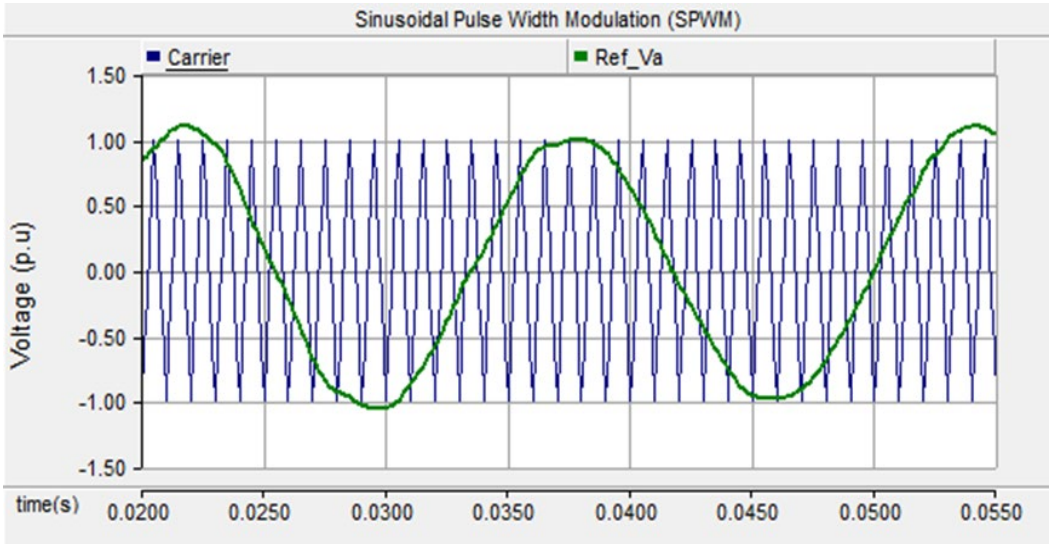


Figure 4. 7: Frequency triangular carrier's waveform is compared with fundamental waveform

CHAPTER 5: RESULTS AND DISCUSSION

This section aims to present the results validating the operation of the developed model illustrated in Figure 5.1 and also indicate the implemented fault points and measuring points. The model is tested during the steady-state condition, and then it's tested during the pole-to-ground condition in different locations. The fault analysis will be carried out to see the effect of a dc fault on MTDC converters and contribution from the system components. The focus will be based on the current (I) kA, Active power (P) MW, and dc voltage (Vdc) kV of the system. During steady-state conditions, there is a power (P) exchange between the converters when a dc voltage is kept at rated value.

In an attempt to explain the steady-state and transient performance of such an arrangement, the test model in Figure 5.1 is simulated under the following operation conditions:

- Under steady-state conditions, VSC 2 inject power at 200MW to VSC 3 and at t=5.0 s power is reversed, and
- at t=6.5 s, a pole-to-ground through 5Ω fault resistance is applied between Converter VSC1 (10 km) and VSC 2 (90 km)

To illustrate the basic behavior and functionalities of the VSC-MTDC type HVDC grid, an example that simulate 400 kV dc-link voltage is presented. VSC 2 and VSC 3 are responsible for controlling power in the system. Initially, VSC 2 generates active power (rectifier operation), and VSC 3 absorbs (inverter operation) the same amount of power generate (200 MW), and at time t=5.0 s, the VSC is commanded to reverse the power flow from 200 MW to -200 MW. Consequently, VSC 1 and VSC 4 are responsible for keeping the grid voltage at a nominal value throughout the simulation.

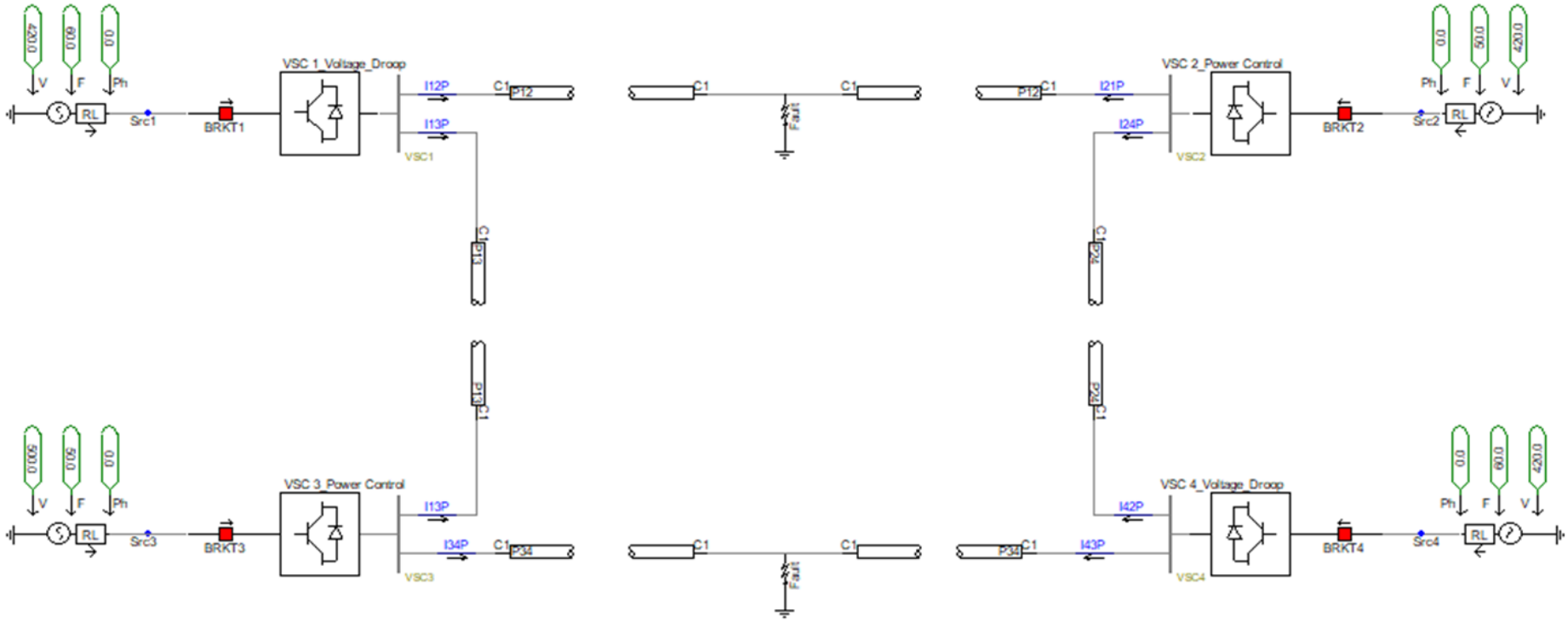
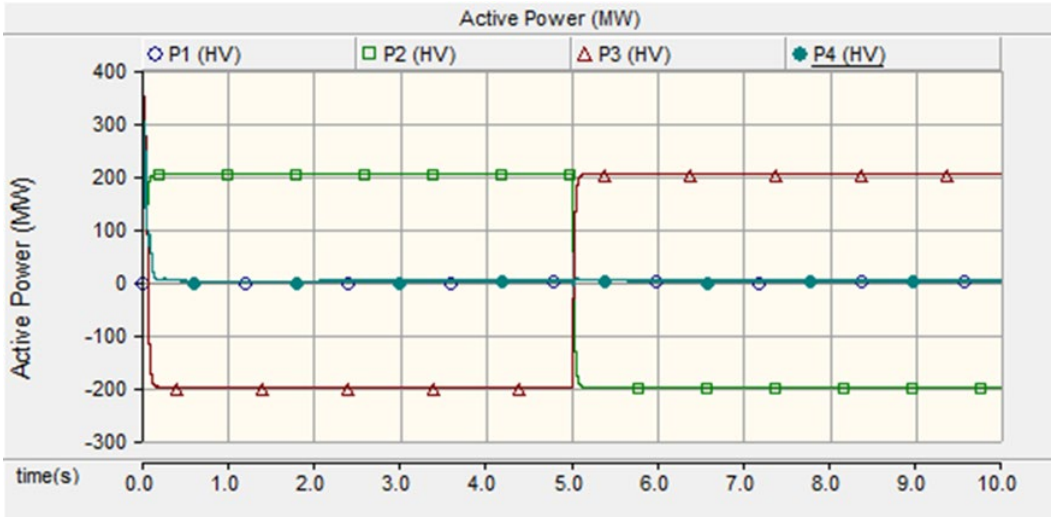


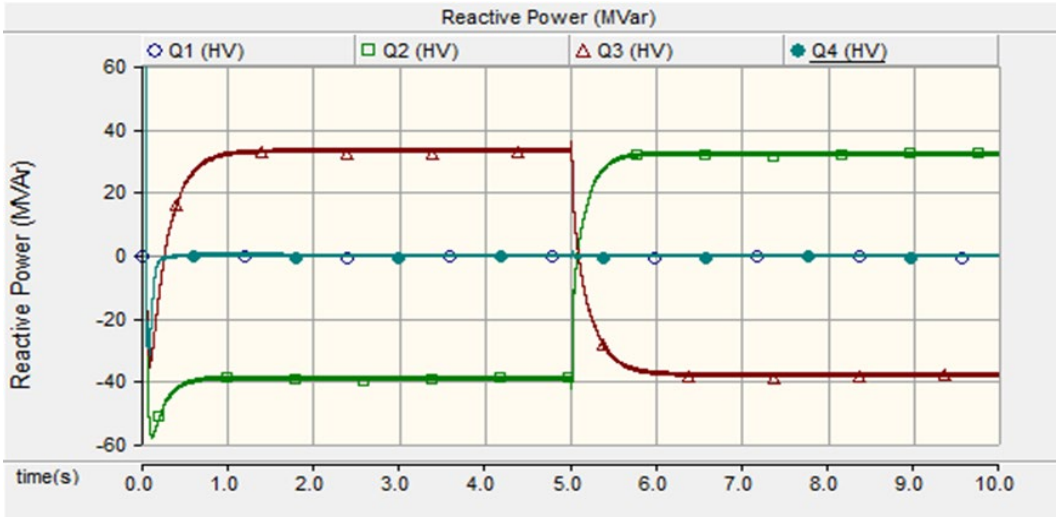
Figure 5. 1: Layout of the VSC-MTDC networks with ground fault.

5.1 Steady-state operation of MTDC

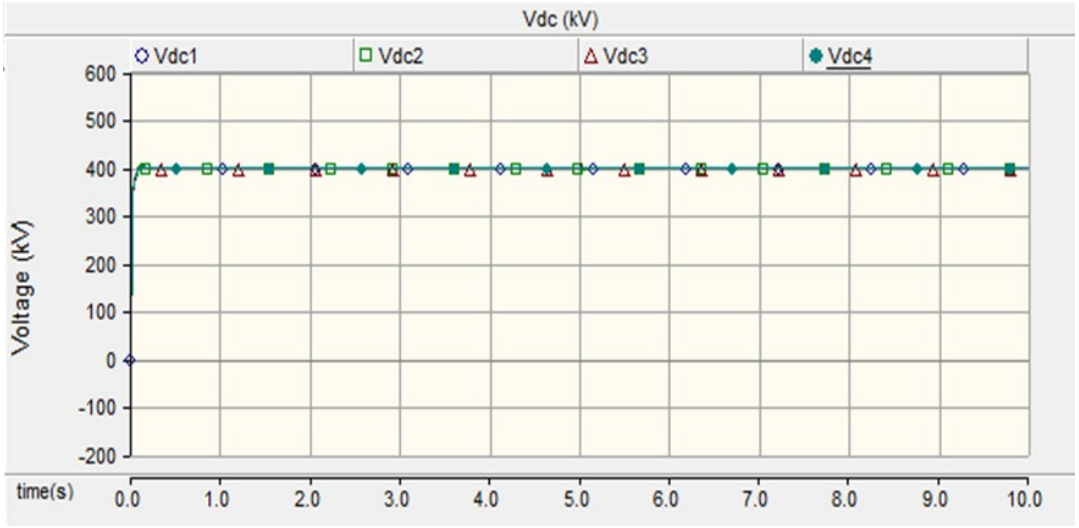
Figure 5.2(a-d) displays the results that illustrate the behavior of the VSC-MTDC grid during power reversal and voltage support. Figure 5.2 (a) and (b) show VSC 2 and VSC3 exchange active and reactive power respectively while VSC 1 and VSC 4 are focusing on regulating the dc voltage and remain with a reference power of 0 MW. Also, both VSC 2 and VSC 3 converters adjust their reactive power exchange with the grid in order to maintain constant grid voltage as shown in Figure 5.2 (c), and Figure 5.2(d) shows voltage for both positive and negative polarity maintained at the nominal value.



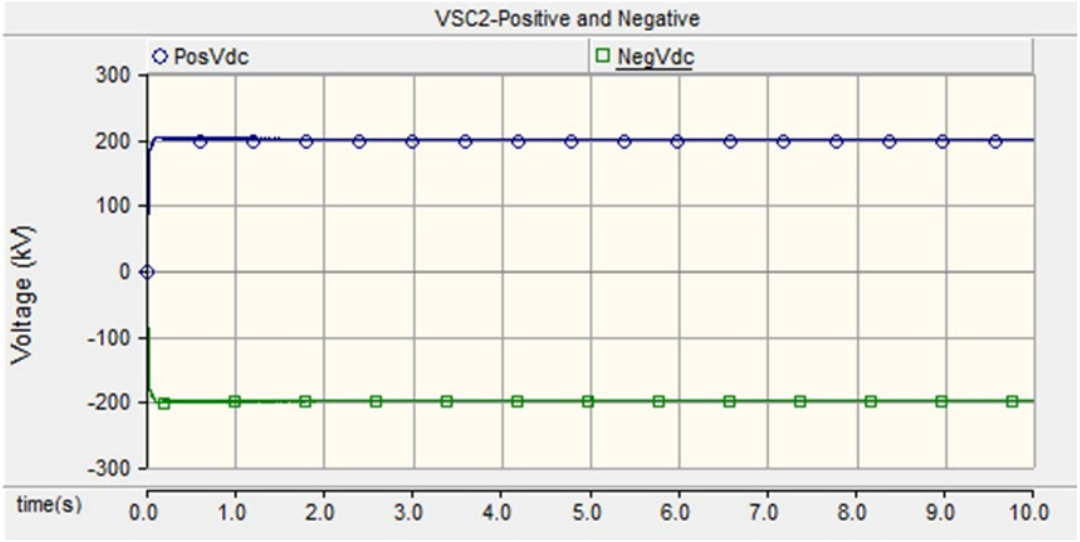
(a) Active power waveform



(b) Reactive power waveform



(c) DC grid voltage waveform in all 4 terminals.

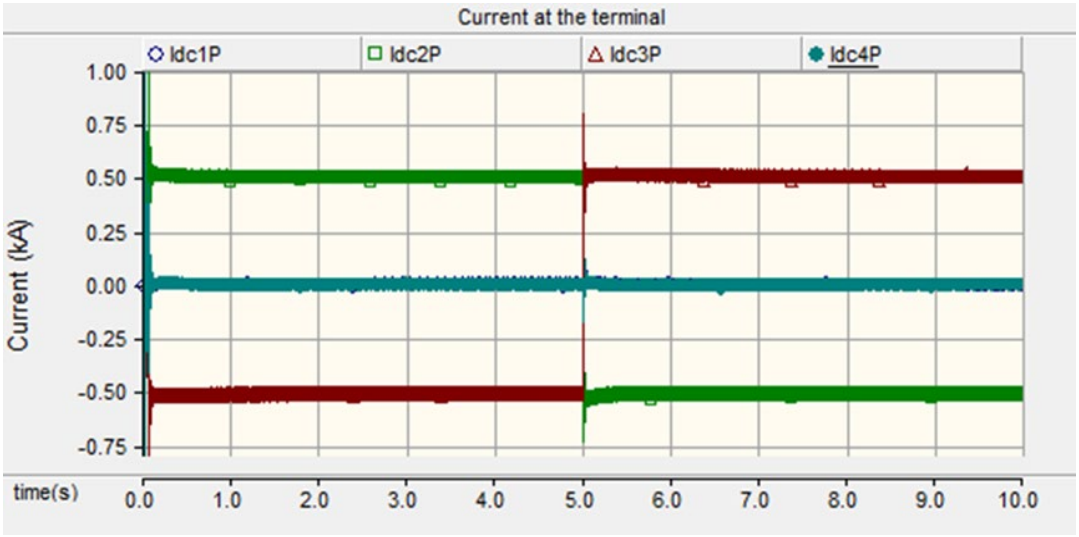


(d) DC grid voltage waveform in each pole.

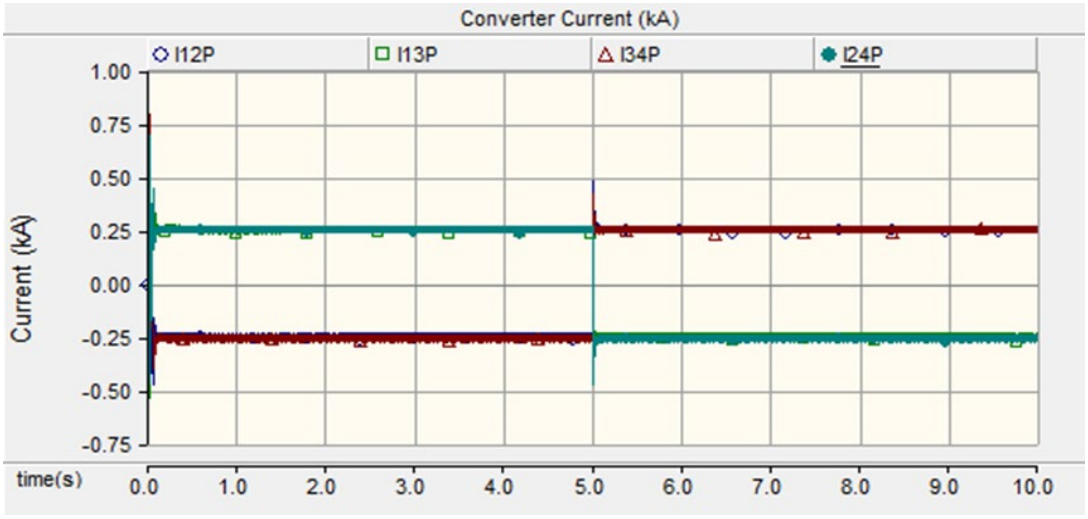
Figure 5. 2: Simulated waveforms during the steady-state condition.

Figure 5.3(a-c) shows current waveforms from the converter VSC2 and VSC3 to the grid. From Figure 5.1, it can be observed that there is no direct connection between power-controlled converters. DC cable is further used to interconnect the converters and transmit the power, and they also connect VSC1 and VSC4. Due to the nature of grid topology chosen for this network, current from VSC2 will flow from the dc cable connecting VSC2 and VSC1 (I_{12}) and cable connecting VSC 2 and VSC 4 (I_{24}). It is the same process with VSC3, where it is joining VCS1 and VSC 4. In Figure 5.3 (a), the current 0.5 kA

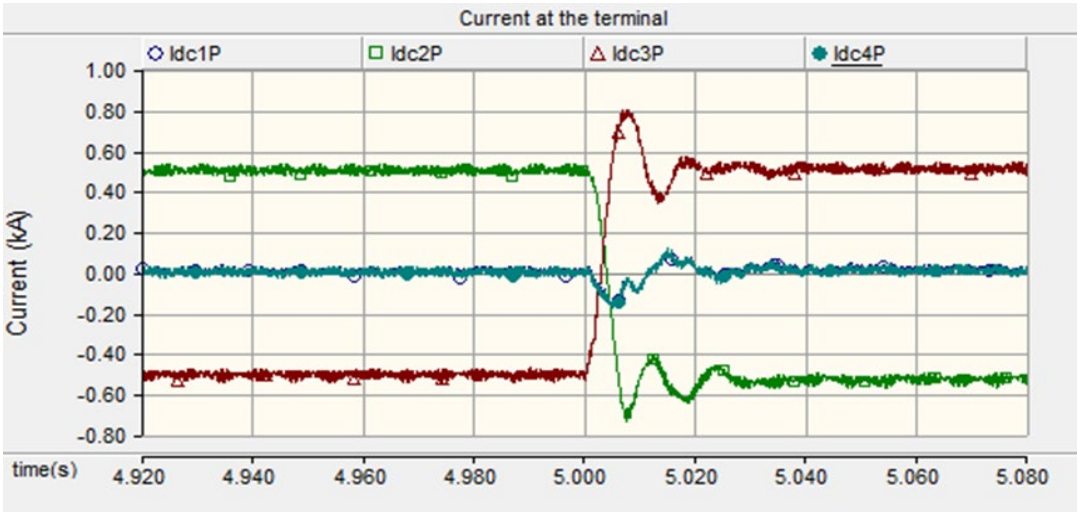
measured from VSC 2 bus (I_{dc2P}) is equal to the total sum of current measured between cable I_{12P} = -0.25 kA and cable I_{24P} =+0.25 kA as shown in Figure 5.3 (b). Figure 5.3 (c) is the zoom version of the current waveform from Figure 5.3(a); it clearly shows the power exchange between the two converters.



(a) Measured current from the bus terminal.



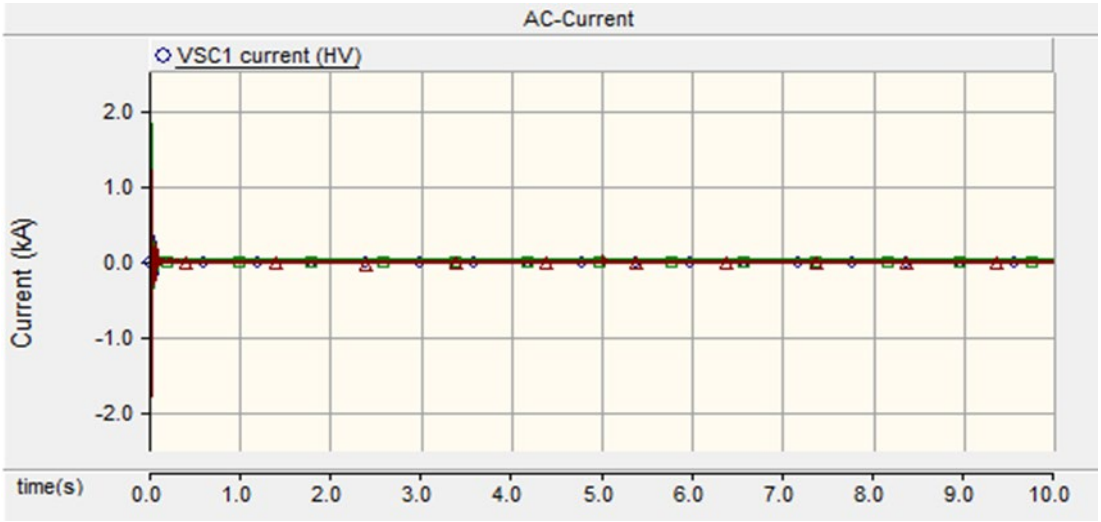
(b) Measured current from the dc cables.



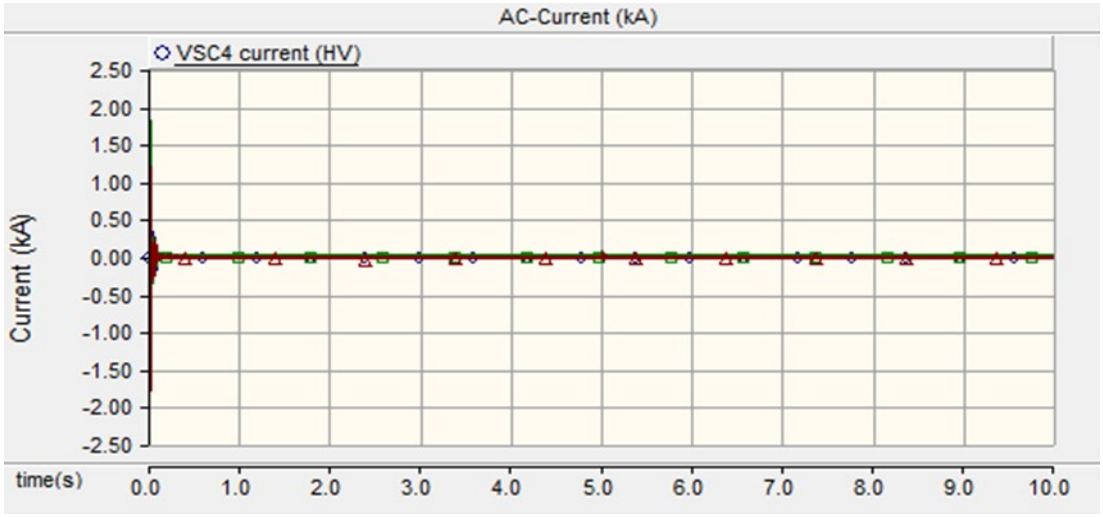
(c) Zoomed measured current from the bus terminal.

Figure 5. 3: (a) Measured current from the bus terminal and (b) dc cables.

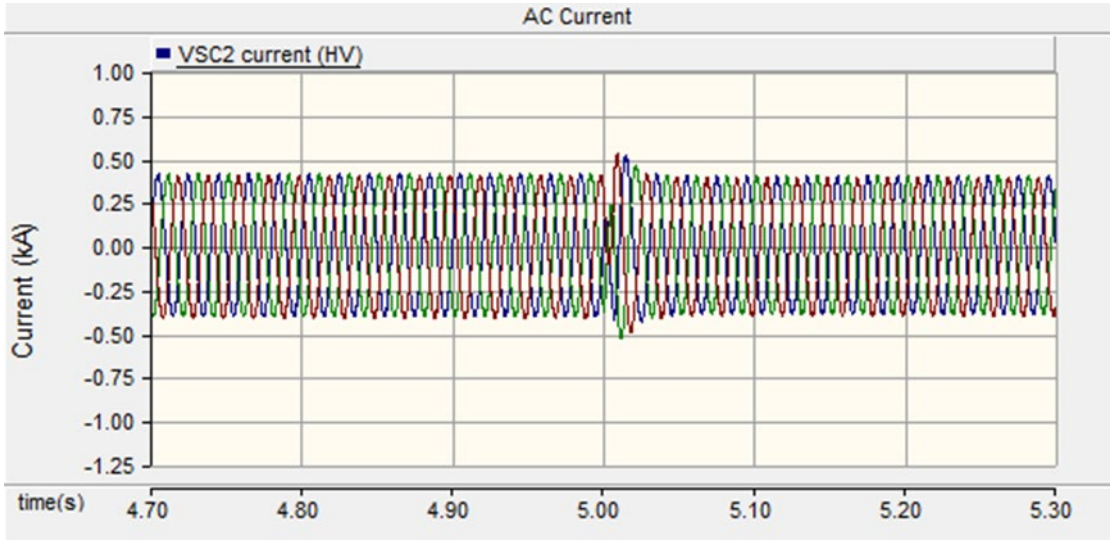
Figure 5.4(a-d) shows the ac currents for each converter at the PCC during the entire operation. The current injection for converter VSC1 and VSC 4 remain at 0 kA, as shown in Figure 5.4 (a-b). Converter 2 and 3 displayed in Figure 5.4 (c-d) show current injection, and it can be observed that at t=5 s, the current is also affected due to power exchange.



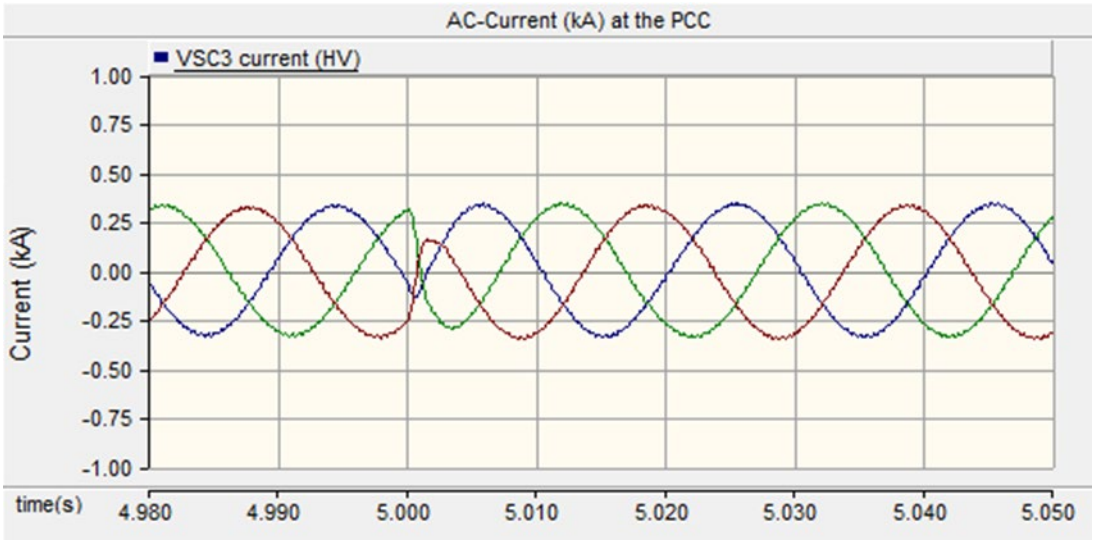
(a) AC current from ac grid to converter VSC1



(b) AC current from ac grid to converter VSC4



(c) AC current from ac grid to converter VSC2



(d) AC current from ac grid to converter VSC3

Figure 5. 4: AC current from the grid.

Figure 5.5 shows the distorted VSC1 capacitor current with both ac components and dc components. The current at this stage contains high harmonics, which leads to ripples. In the literature, one of the disadvantages that are facing two-level topology is high harmonics.

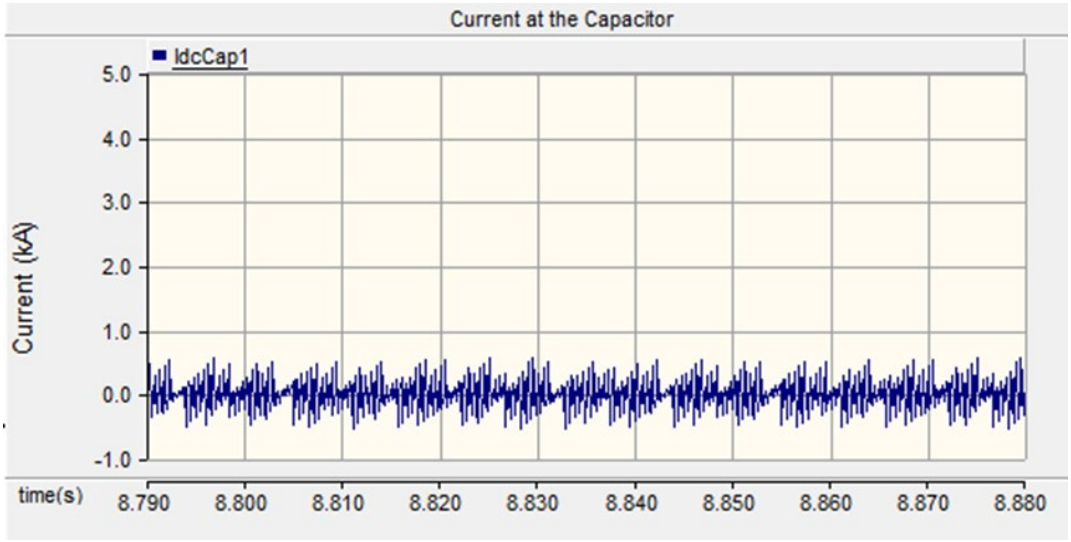


Figure 5. 5: Capacitor current

Figure 5.6 shows converter diode conduction current for each diode under normal conduction. The current is approximately ±0.5 kA.

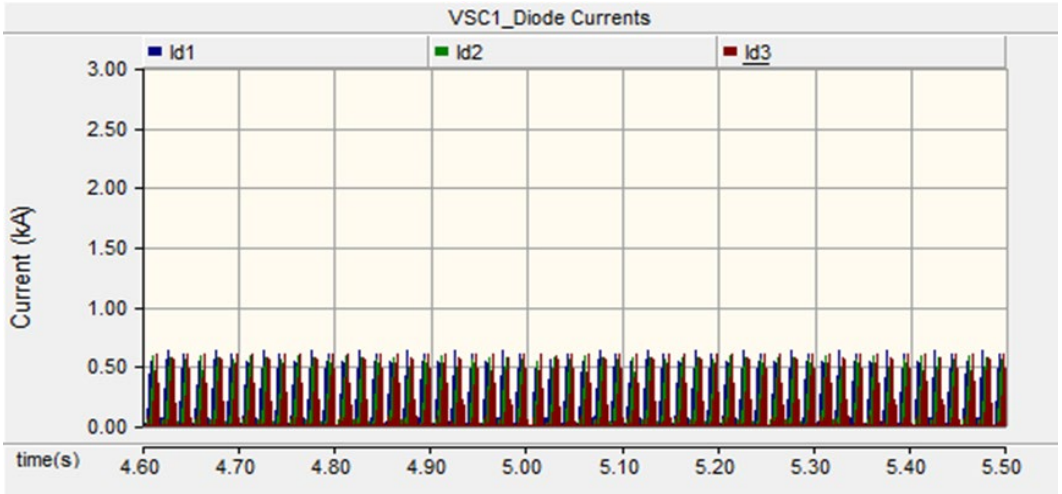


Figure 5. 6: VSC1 diode currents

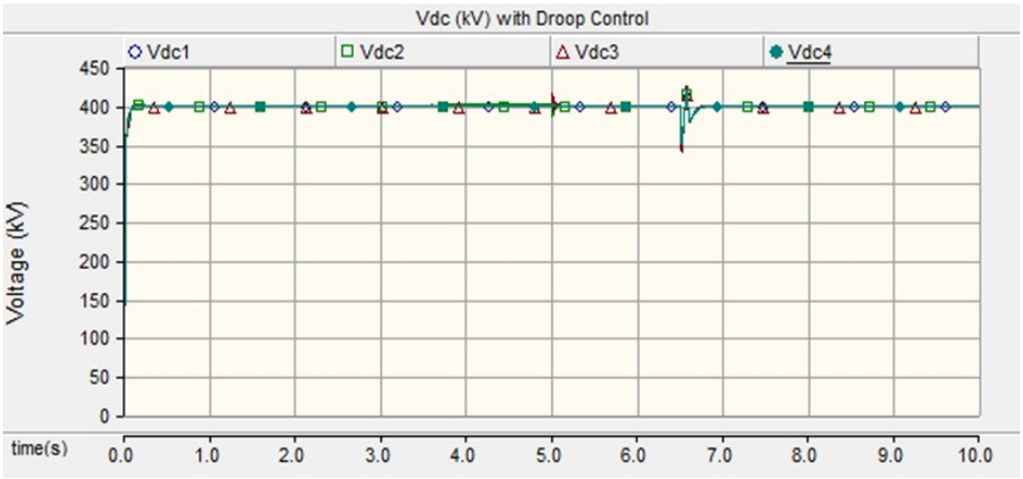
5.2 DC network faults

5.2.1 Evaluation of the transient response of pole-to-ground dc fault on a mono-polar MTDC when a fault is applied 10km and 50km away from VSC1.

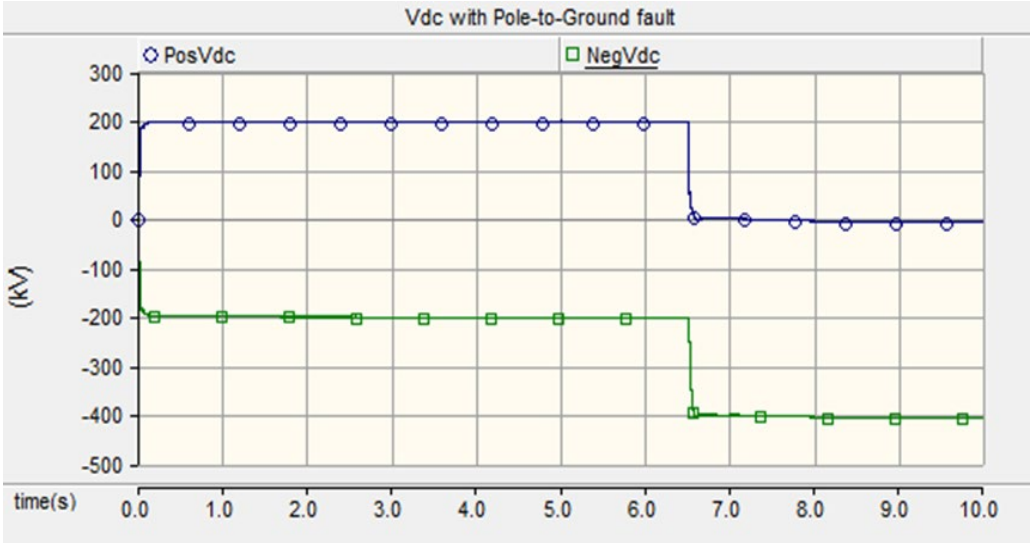
5.2.1 (a) Pole-to-ground fault with Droop control strategy

To assess the response of the four-terminal symmetrical VSC-HVDC grid to dc side faults, the model tested in Figure 5.1 is subjected to pole-to-ground fault dc network fault at a distance10 km away from VSC1, the cable connecting VSC1 and VSC2 through fault resistance of 5 ohms at t=6.5 s. In this test model, the voltage-droop control strategy discussed in the literature is implemented in VSC1 and VSC4, in order to regulate the dc voltage and keep it at the nominal value. The voltage drop can be seen in Figure 5.7 (a), but the change in dc voltage quickly settles back to the rated value. The voltage in each pole is shown in Figure 5.7 (b), where the negative pole reaches 400 kV leaving the faulty line at zero as it is shorted to ground.

From the literature, when the fault occurs in the symmetrical system, the health pole will be exposed to full dc-link voltage, as shown in Figure 5.7 (b), if both cable are rated to full dc voltage. Under this condition, the converter will operate as an asymmetrical monopolar, and it will continue to exchange the active power to all the converters. However, this arrangement may not be economically feasible in the real world system applications of the VSC-HVDC.



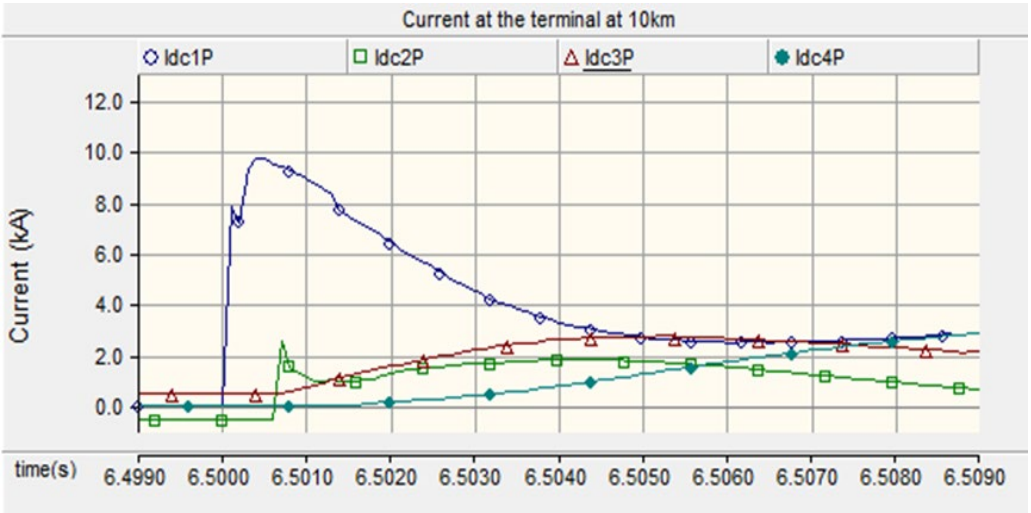
(a) DC voltage during dc fault



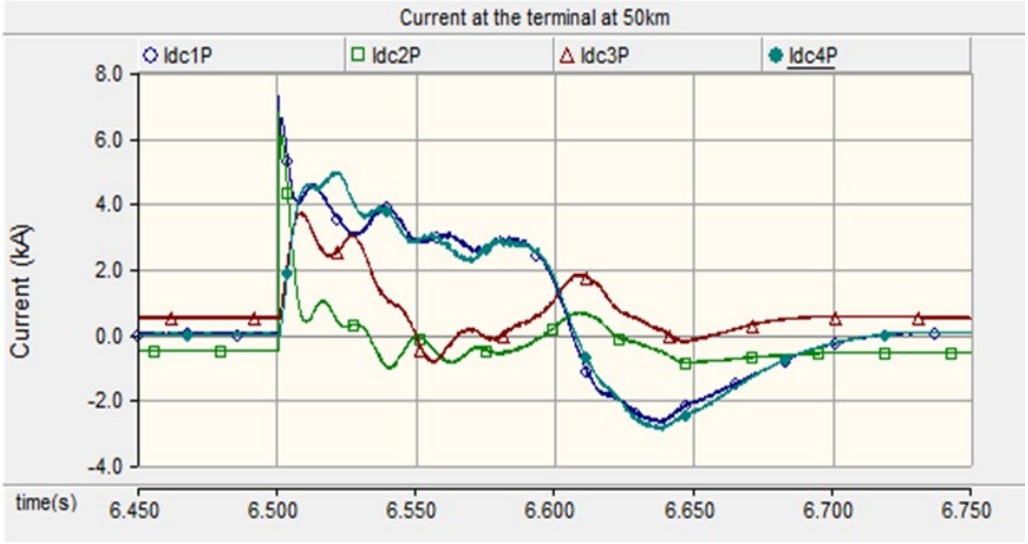
(b) DC voltage in each pole

Figure 5. 7: DC link voltage measured for all terminals.

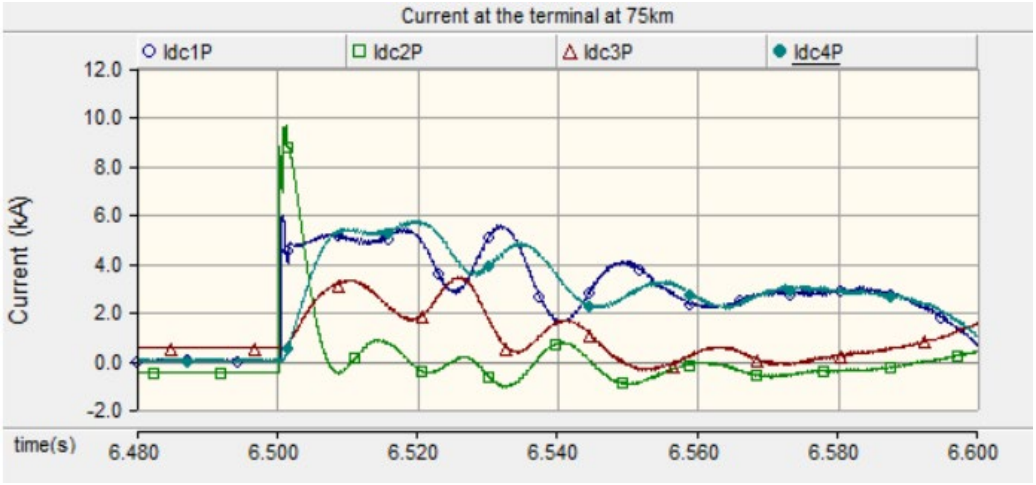
The ground fault is inserted 10 km away from VSC1, and the fault current measured at the terminal is shown in Figure 5.8 (a), and the peak fault current is ± 9.9 kA. Figure 5.8 (b) shows the difference in fault current when the ground fault is introduced at a distance 50 km away from VSC1. The fault current measured to be ± 7.8 kA; these results show the effect of varying the distance during the ground fault. Furthermore, it is assumed that the fault current magnitude will be smaller if the ground fault is introduced further away from 50 km. Figure 5.89 (c) shows the fault current magnitude when the fault is inserted close to VSC 2, where its 75 km away from VSC1. Compared to other converters, VSC 2 fault current magnitude is almost ± 9.5 kA.



(a) DC fault current measured 10km away from VSC1.



(b) DC fault current measured 50 km away from VSC1.

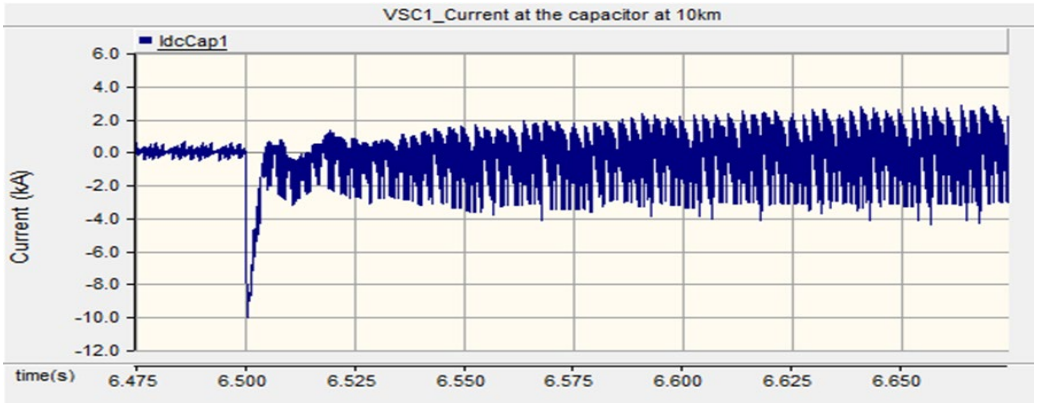


(c) DC fault current measured 75 km away from VSC2.

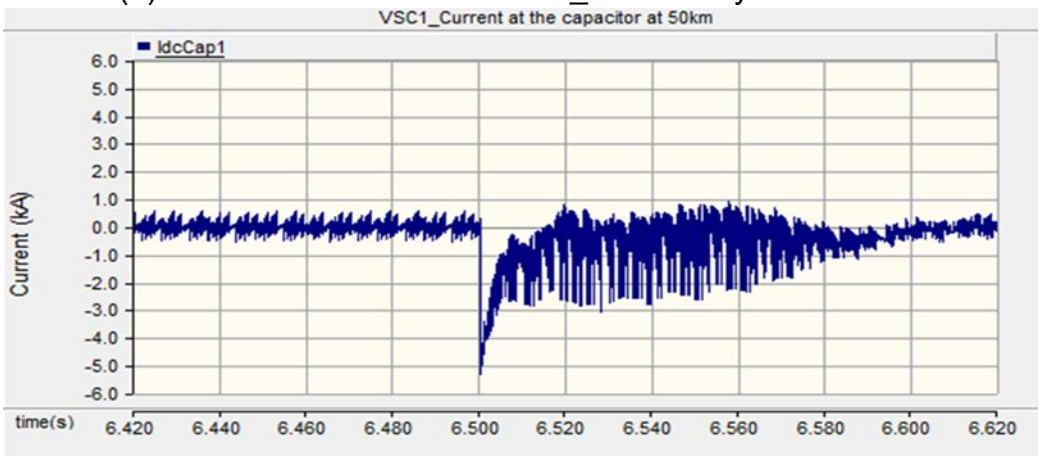
Figure 5. 8: DC currents during the pole-to-ground fault.

The significant rise in dc fault current in the capacitor, as shown in Figure 5.9 (a-c), is caused by the immediate drop of voltage in the positive pole. Figure 5.9(a) is the fault current measured at 10 km away, whereas Figure 5.9 (b) shows the current measured at 50 km away from VSC1. The converter dc-link capacitor for the tested model is earthed at the center causing high currents during the ground fault. Figure 5.9 (c) shows the impact of ground fault when the earthing point in the dc-link capacitors is eliminated to the circuit. The change in current can be noticed as when compared to Figure 5.9 (a) where

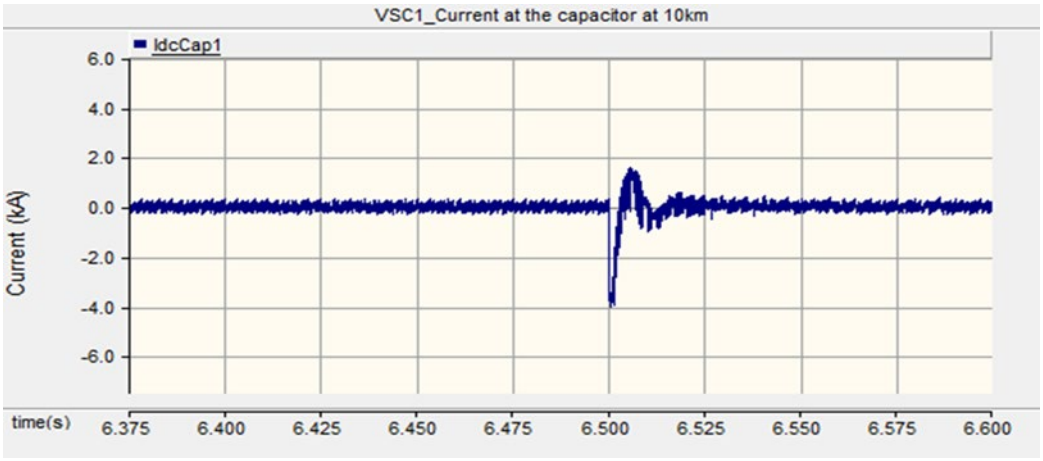
fault current measured is very high (±9.9 kA), and Figure 5.9 (c) is estimated to be (±4 kA). Also, Figure 5.9 (c) shows how fast capacitors can discharge compared to Figure 5.9 (a). However, the absence of earth in the dc-link results in periodic oscillations of currents flowing in the system.



(a) DC link current without earth_10km away from VSC1.



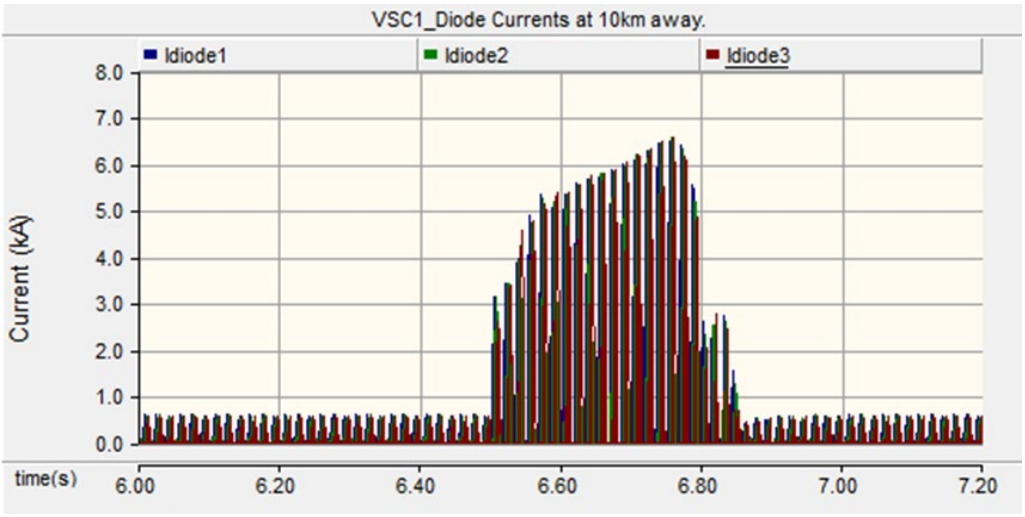
(b) DC link current with earth_50km away from VSC1.



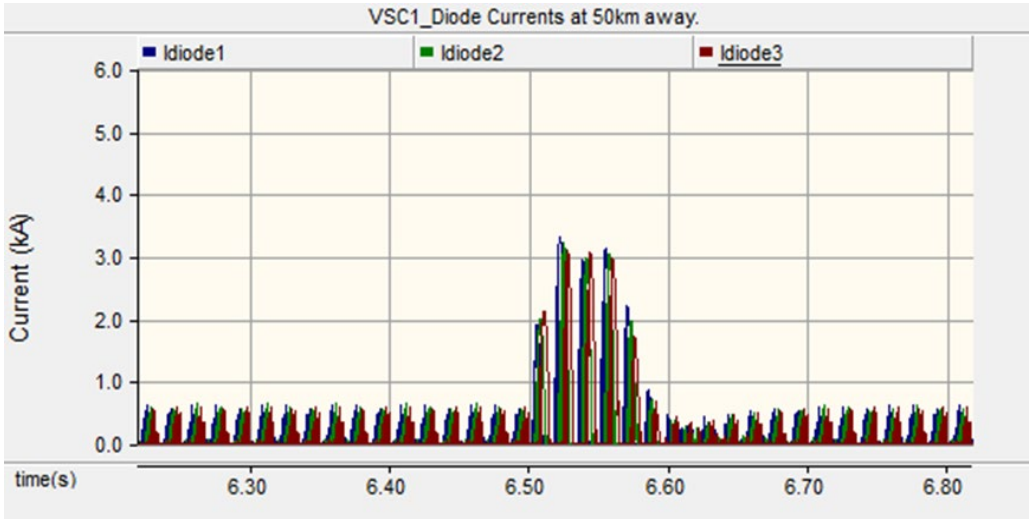
(c) DC link current without earth_10km's away from VSC1.

Figure 5. 9: Simulated waveform of dc-link capacitors during the pole-to-ground fault.

During dc faults, anti-parallel diodes are the most vulnerable devices in the converter, whereas IGBTs block themselves for protection. The fault current passes through the anti-parallel diode as they will form rectifier-bridge. This exposes anti-parallel diodes to high current magnitude, and they exceed the maximum current rating. Figure 5.10 (a-b) shows the fault current flowing through the diodes. Figure 5.10 (a) shows the fault current when the fault occurs close to the converter terminal, and Figure 5.10 (b) shows fault current when it's 50 km away from VSC1 and the effect of the distance.



(a) Anti-parallel diode current measured 10km away VSC1.

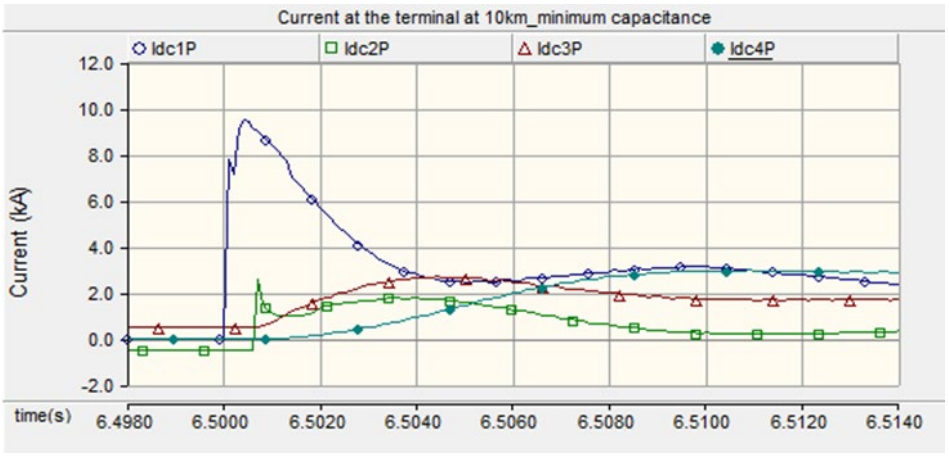


(b) Anti-parallel diode current measured 50km away VSC1.

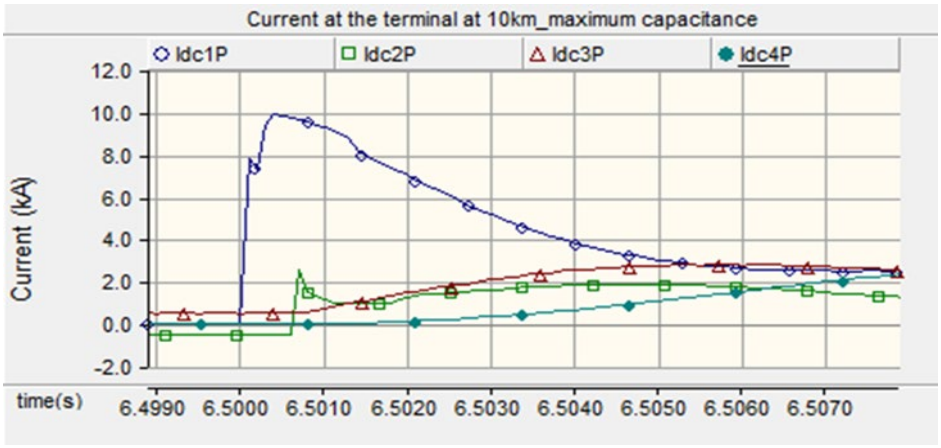
Figure 5. 10: Converter anti-parallel diodes during a ground fault.

5.2.2 Significance of varying the dc capacitance to ±5%

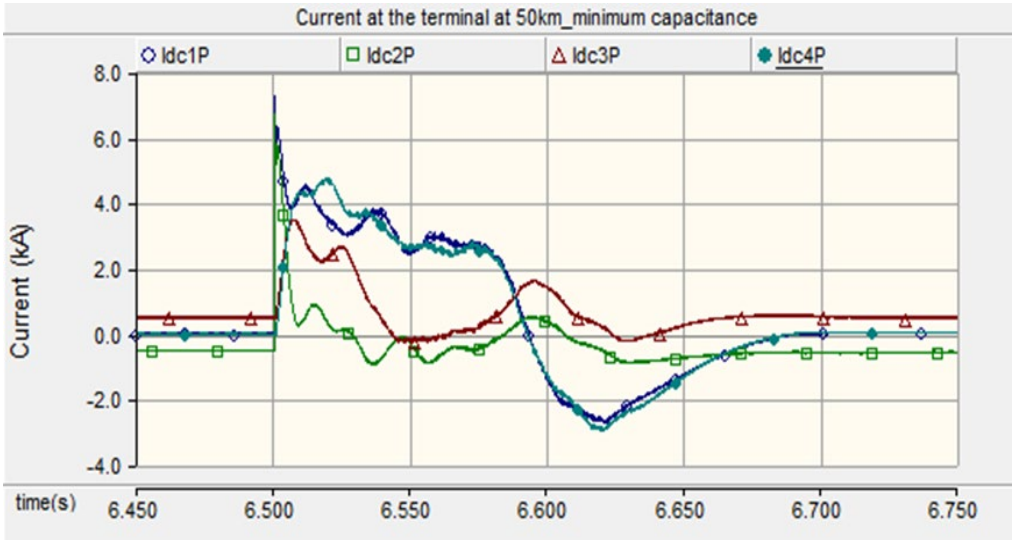
The main factors that affect the rate of the current rise in the converter dc-link capacitor during fault are fault impedance, cable impedance, ac filter, and dc-link capacitance. From the literature, dc-link capacitors are used for filtering and keeping the dc voltage constant and can be calculated using equation (2.4). The significance of varying the dc capacitance to ±5% as a minimum and maximum rating of the converter is shown in Figure 5.11(a-d), and the change in peak current can be seen in Figure 5.11 a and 5.11 c for both minimum and maximum capacitance when the fault is 10 km and 50 km away from VSC1. The results show that the minimum capacitance discharges very quickly, and the fault peak current is reduced. The opposite is seen in Figure 5.11 b and 5.11 d, where maximum results are presented. Both maximum and minimum have their own advantages and disadvantages, such as signals with a high level of noise, low dc filtering, and loss of constant dc voltage.



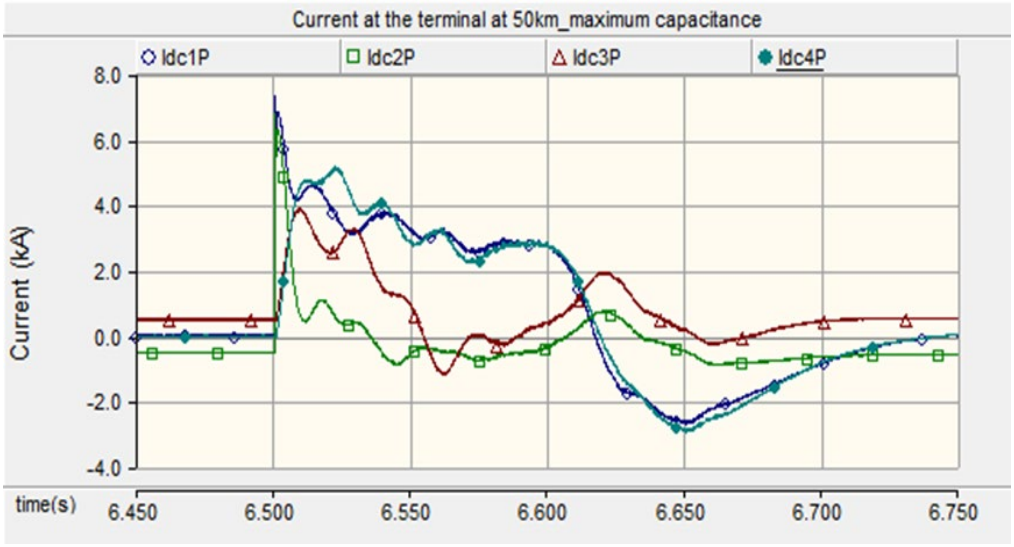
(a) Measured dc current at 10km at minimum capacitance.



(b) Measured dc current at 10km at maximum capacitance.



(c) Measured dc current at 50km at minimum capacitance.



(d) Measured dc current at 50km at maximum capacitance.

Figure 5. 11: DC current measured for maximum and minimum capacitance.

5.3 Chapter Summary

During dc-side fault analysis, a pole-to-ground fault was taken into consideration as it's more likely to occur, although it is less severe compared to pole-to-pole. The following were observed during the steady-state analysis: the dc voltage in the grid was maintained at the rated value 400 kV, the currents measured at the converters bus was 0.5 kA, and the current flowing through the cables was 0.25 kA. Under the fault condition, the dc voltage drop needs to be maintained to a closed range to avoid the grid to collapse. The

voltage droop technique was incorporated in the dc voltage controller to keep the dc voltage at the narrow range.

Depending on the value and nature of ground fault resistance, the fault current magnitude varies, and distance variation along the cable has a significant contribution in the fault current. It is observed that fault close to the converter (10 km measured ± 9.9 kA) results in high fault currents compared to fault away from the converter (50 km measured 7.8 kA). As much as other converters are affected, but their measured currents are very much lower when compared to the converter close to the fault location. This clearly indicates that the protection of this system needs to have a high level of selectivity and detection.

Throughout the analysis, the converter side uses low impedance earth, which is categorized as the solid earth. The earth was then removed to analyze the effectiveness or significance of the earth. It was observed that the converter without earth yields lower fault current, but the absence of earth in the dc-link results in periodic oscillations of currents flowing in the system. Whereas, the earthed converter generates higher fault current, and the discharge current takes longer to return to steady-state, but the grid currents have minor oscillations.

Since dc-link capacitors are considered as one of the main factors affecting the rise of fault current magnitude, an analysis was carried out when the capacitance was varied to the maximum and minimum capacitance that the system can take. It was varied to ±5% (250 uF and 350 uF), and the results showed that the fault current is reduced, but it discharges very quickly, and when the 350 uF were inserted, the results showed that the fault current was much higher, but it takes longer to discharge. The best size of the capacitors can be selected based on the priority. Both maximum and minimum hold its own advantages and disadvantages, such as signals with a high level of noise, low dc filtering, and loss of constant dc voltage.

CONCLUSION

Transient dc-side fault analysis in a two-level monopolar VSC-based MTDC HVDC scheme consisting of four asynchronous terminals is studied. For MTDC networks to become a reality, several technical issues need to be addressed to ensure stable and safe operation. One of the main challenges that need to be addressed is the protection of VSCs during dc-side faults, as it poses a severe threat to the VSC-HVDC MTDC networks. Unlike conventional LCC-based HVDC transmission topology, which does not suffer from a high level of dc-side fault overcurrents, VSCs experience a large amount of fault current from the dc-side fault. These high fault currents are the contribution of capacitor-discharge, and an ac-side current flowing through anti-parallel diodes.

In point-to-point VSC-based system, ac circuit breakers are used to disconnect the faulted line, and this isolates the dc system entirely. On the other hand, MTDC systems involve large transmission capacities, and the application of ac breaker is not a viable option. In MTDC, it is essential to quickly and reliably detect and isolate only the unhealthy line from the network in order to protect the sensitive power electronics and, most importantly is to ensure the security of supply. Presently, the traditional protection techniques implemented in the VSC-HVDC MTDC networks do not meet the dc characteristics. It is, therefore, necessary to study the behavior of converter under fault conditions in order to design and develop the best protection for the network.

From this study, the following summary and conclusions can be drawn:

- An in-depth theory of different VSC-based HVDC transmission systems has been revised in the literature review.
- A VSC-based HVDC-MTDC system has been modelled using PSCAD engineering software tool comprising of four meshed monopolar, two-level VSC-HVDC converters interconnected into a dc-grid.
- Line model specification for transient faults analysis in the network was carefully selected in the PSCAD software package.

- The influence of the components main parameters on the transient fault current development during pole-to-ground faults, as well as the interaction between these components by means of simulations, was analyzed in the MTDC system.
- The behavior of a two-level voltage source converter in an MTDC network, connected in a radial grid topology during the pole-to-ground fault, was studied.
- For the power delivery system, network topology, and grounding scheme, the factors influencing fault current were identified and quantified.

The simulations were carried out with the main aim of analysing the transient faults currents in the MTDC network and study the behaviour of the converters under fault condition. From the research questions, the following conclusion were drawn:

- Power-sharing between VSC 2 and VSC 3 was balanced with insignificant disturbance during fault and the power controller kept the two converters at their rated power, since power control was assigned in VSC 2 and VSC3. The voltage controlled converters manage to keep the grid voltage at the narrow range during the fault, however the power for these two converters was not controlled and during fault period, the power was much higher than it normal rating.
- Main components such as anti-parallel diodes may be highly affected by the high currents faults from the dc-side and the contribution from the ac-side depending on its rating. The IGBT switches normally block themselves for protection, but they might be affected by the fault currents. The cable insulation could be damaged.
- Fault location has a huge impact in the nertwork. If the fault is close to the converter station, the magnitude of fault current will be higher compared to when the fault is away from the converter. Suitable dc fault detection and location techniques are essential to provide protection for MTDC nertwork.

From the results, it was observed that the dc-link capacitor has a considerable contribution to the fault current. The first peak current that results from the capacitor only lasts for few milliseconds, and it falls back, and then eventually, it reaches a steady-state due to the negative pole (healthy) handling the full dc-link voltage. Initially, positive and negative poles carry 200 kV each, and during the fault, the positive pole is grounded, and the negative pole is subjected to full rating.

The protection design of the VSC needs to be able to detect whether its ground fault or short circuit since the location of the fault needs to be identified and repaired. Another observation made when the fault is inserted at a distance 50 km away from the converter, meaning the fault is at the center of the two converters, the outcome results in high currents in both converters. The isolation of the fault should be selective. The dc circuit breakers are mostly recommended to be used as primary protection; however, different protection techniques need to be incorporated with dc circuit breaker in order to quickly identify, select and reliably isolate the faulted line. Moreover, the protection should be able to isolate the line before the fault reach the maximum fault current in order to avoid the damage in the converter components.

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