



# **Voltage Stability in Distribution Network.**

by

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## **DEDICATION**

I dedicate this work to my father Dr Sambo to whom my dreams live.

## DECLARATION OF AUTHORSHIP; PLAGIARISM

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## PUBLICATIONS

DETAILS OF THE CONTRIBUTION TO PUBLICATIONS that form part/or include research presented in this thesis (include publications in preparation, submitted, in press and published and give details of the contributions of each author to the experimental work and writing of each publication).

Publication 1: **Sboniso B Masikana, Gulshan Sharma, Kayode Akindeji and Innocent Ewean Davidson**, "Voltage stability enhancement studies for distribution network with installation of FACTS," in *2020 International Conference on Artificial Intelligence, Big Data, Computing and Data Communication Systems (icABCD)*, 2020: IEEE., Durban, 6-7 Aug 2020.

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## ABSTRACT

Voltage stability studies and to maintain the flat voltage profile is quite important in order to maintain the healthy operation of electric power network as well as to provide the quality and cheap electric energy to the modern power users. Further with the advancement of power electronics technologies and its application to design flexible alternating current transmission devices (FACTS) have made it easier to alleviate the voltage stability problem in a quicker and cheaper way in the modern DNs. Therefore, this research work shows an attempt to investigate and solve the problem of voltage instability in the distribution network (DN) with the help of FACTS. All buses and lines are calculated in terms of voltage stability index (VSI) and to identify the optimal location of FACTS. The bus or line with minimum voltage profile in terms of VSI are more sensitive to the voltage collapse and it may further lead to blackouts. Hence, the FACTS are permanently installed at the weakest point to enhance voltage profile and improve the voltage stability in the DN. The present study is tested on standard IEEE-15 bus DN and application results are shown to verify the feasibility of the present studies for DN.

The beauty and future promise of UPFC in power quality improvement was authenticated on the IEEE-15 bus DN carried out using *MATLAB* software tool, five different scenarios were considered by increasing the load up to 40% at an interval of 10% from its nominal operating load. With the aim of determining the impact of UPFC on bus voltage and system losses, the load flow analysis was contributed on each scenario with and without UPFC placement in the DN. After UPFC placement there was a significant enhancement of voltages of all busses as well as weakest bus voltage jump from 0.5750 to 0.9750 p.u. and shifting that bus as well as system from voltage instability to stable zone. The active and reactive power losses were decrease by 9.83% and 27.27% that fulfil the beauty of the UPFC installation in the DNs as well as it promise to mitigate the voltage instability problem of the modern DNs

***Keywords— Voltage profile, VSI, FACTS, power losses, distribution network.***

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## ACRONYMS

|                  |                                                  |
|------------------|--------------------------------------------------|
| AC               | Alternating Current                              |
| AVR              | Automatic Voltage Regulator                      |
| DC               | Direct Current                                   |
| DG               | Distributed Generator                            |
| DN               | Distribution Network                             |
| D-STATCOM        | Distribution Static Synchronous Comparator       |
| E-STATCOM        | Energy Storage Static Synchronous Compensator    |
| FACTS            | Flexible Alternating Current Transmission System |
| FLC              | Fuzzy Logic Controller                           |
| FVSI             | Fast Voltage Stability Index                     |
| G-S              | Gauss-Siedel                                     |
| HVDC             | High Voltage Direct Current                      |
| IEEE             | Institute of Electrical and Electronic Engineers |
| IGBT             | Insulated Gate Bipolar Transistors               |
| IPFC             | Interlink Power Flow Controller                  |
| KVA              | Kilo-Volt Ampere                                 |
| LMN              | Line Stability Index                             |
| LQP              | Line Stability Factor                            |
| MATLAB           | Matrix Laboratory                                |
| MVA              | Mega Volt Ampere                                 |
| MVA <sub>r</sub> | Mega Volt Ampere Reactive                        |
| N-R              | Newton-Raphson                                   |
| OLTC             | On Load Tap-Changer                              |
| PCC              | Point of Common Coupling                         |
| PLL              | Phase Lock Loop                                  |
| PI               | Performance Index                                |
| POD              | Power Oscillation Damping                        |
| PSS              | Power System Stabilizer                          |
| PU               | Per-Unit                                         |

|         |                                                 |
|---------|-------------------------------------------------|
| PVSI    | Performance Voltage Stability Index             |
| P-V     | Active Power Voltage                            |
| Q-V     | Reactive Power Voltage                          |
| RES     | Renewable Energy Sources                        |
| RP      | Reactive Power                                  |
| SI      | Stability Index                                 |
| SSSC    | Static Synchronous Series Compensator           |
| SPWM    | Sinusoidal Pulse Width Modulation               |
| STATCOM | Static Synchronous Compensator                  |
| SVC     | Static Var Compensator                          |
| TCPAR   | Thyristor Controlled Phase Angle Regulator      |
| TCPST   | Thyristor Controlled Phase Shifting Transformer |
| TCSC    | Thyristor Controlled Series Capacitor           |
| TSSC    | Thyristor Controlled Series Compensator         |
| TS      | Transient Stability                             |
| UPFC    | Unified Power Flow Controller                   |
| VCPI    | Voltage Collapse Point Indicator                |
| VSC     | Voltage Source Converters                       |
| VS      | Voltage Stability                               |
| VSI     | Voltage Stability Indices                       |
| VSL     | Voltage Stability Limit                         |

## NOMENCLATURE

|                 |                                                   |
|-----------------|---------------------------------------------------|
| $A$             | Cross-sectional Area [ $m^2$ ]                    |
| $C$             | Capacitance of the line [ $F$ ]                   |
| $H_z$           | Hertz                                             |
| $I_c$           | Capacitor Current [A]                             |
| $I_{dc}$        | Current of a Direct-current [A]                   |
| $I_L$           | Load Current [A]                                  |
| $I_{sh}$        | Shunt Current [A]                                 |
| $L$             | Inductance [H]                                    |
| $l$             | Length of the conductor [m]                       |
| $P$             | Active power [W]                                  |
| $P_{losses}$    | Power losses [W]                                  |
| $P_{max}$       | Maximum power [W]                                 |
| $P_r$           | Active power at the receiving end [W]             |
| $Q$             | Reactive power [VAr]                              |
| $Q_r$           | Reactive power at the receiving end [VAr]         |
| $q$             | Charge on the conductor [C]                       |
| $R$             | Resistance of the conductor material [ $\Omega$ ] |
| $S$             | Apparent power [VA]                               |
| $t$             | Time-step [s]                                     |
| $V_{dc}$        | Direct-current voltage [V]                        |
| $V_i^*$         | Conjugate voltage [V]                             |
| $V_m$           | Bus voltage at the receiving end [V]              |
| $V_{mag-sh}$    | Injected shunt voltage magnitude [V]              |
| $V_{nom}$       | Nominal voltage magnitude [V]                     |
| $V_{nom}^{lim}$ | Voltage deviation limit [V]                       |

|               |                                                   |
|---------------|---------------------------------------------------|
| $V_s$         | Sending end voltage [V]                           |
| $V_{se}$      | Series voltage source [V]                         |
| $V_{sh}$      | Injected shunt voltage [V]                        |
| $V_R$         | Receiving end voltage [V]                         |
| $V_{ref}$     | Reference voltage [V]                             |
| $V_{reg}$     | Voltage regulation [%]                            |
| $X_L$         | Inductive reactance [ $\Omega$ ]                  |
| $X_q$         | Reactive power compensation [ $\Omega$ ]          |
| $Y_{ii}$      | Self-admittance [U]                               |
| $Y_{ik}$      | Mutual admittance [U]                             |
| $Z$           | Impedance of the line [ $\Omega$ ]                |
| $Z_{sh}$      | Shunt impedance [ $\Omega$ ]                      |
| $Z_{se}$      | Series impedance [ $\Omega$ ]                     |
| $\omega$      | Angular frequency [Wb]                            |
| $\delta_R$    | Bus angle at the receiving end [degree]           |
| $\delta_s$    | Bus angle at the sending end [degree]             |
| $\rho$        | Resistivity of the conductor [ $\Omega\text{m}$ ] |
| $\lambda$     | Instantaneous flux linkage [Wb]                   |
| $\alpha - sh$ | Theta [degree]                                    |
| $\Sigma$      | Sum                                               |
| $\theta$      | Line impedance angle [degree]                     |



# CHAPTER ONE

## INTRODUCTION

### 1.1 Background

In vertically incorporated utility structure, all elements, including; generation, transmission and distribution of electrical power are within the aegis of focal vitality the executives' organization. Power generation is carried out to accomplish the least operational expense and power distribution companies are making the final delivery of electrical power to the consumers. Due to continuous advancements, the consumers' demands keep increasing exponentially. Consequently, the power system network face many problems such as; voltage and frequency instability, line overloaded and power system blackout. Voltage collapse is a process in which the appearance of sequential events together with the voltage instability in a huge area of system can lead to the case of low voltage condition in the network [1]. Load increasing can prompt unnecessary interest of reactive power; the system will indicate voltage instability. In the event that there are not adequate reactive power assets and the excessive demand of reactive power can prompt voltage collapse. To overcome voltage instability due to power system configuration, topology can be modified by adding shunt capacitors and FACTS devices at the suitable locations [2]. This research work addresses the static modelling of a Unified Power Flow Controller (UPFC), and its abilities to improve the voltage profile and bus power flow to that it is associated. This power electronic device technology is referred to as FACTS technology; This allows greater controllability and increases the operation of the transmission network in terms of power flow, The stability limits for current power systems with advanced control technologies [3, 4]. Among different types of FACTS, UPFC is capable of controlling both the active and reactive power flow of the network simultaneously, in addition, factors that affect the power flow through the network such as; voltage magnitude, impedance and phase angle in UPFC are controllable [5]. The placement and sizing strategy of shunt FACTS controller using Real Coded Genetic Algorithm was proposed to maintain voltage stability in [6]. Another approach of enhancing the voltage stability by placing FACTS devices in the weakest bus or lines of the power system which are closest to experience



voltage collapse. Different methods like P-V curve, Q-V curve and index based methods have been utilized to find the locations for FACTS devices. P-V curve was used in [7]- [8] to determine weakest bus for FACTS devices allocation. In [9], the stability of load flow technique was studied by the authors for the distribution system. The real-time contingency evaluation and ranking technique was discussed in [10] for DNs. In [11], the authors have presented the analysis and voltage stability solution for bulk power system. In the view of above discussion, this research work is set to:

- (a.)To study the voltage stability issues of the distribution network (DN). The standard IEEE 15 bus system is used for the analysis and to study the voltage stability of the DN.
- (b.)The models of voltage collapse point indicator and line stability factor is modelled and simulated to carry out the present studies. The various loading cases are considered in order to identify the exact bus which may bring the voltage instability in the DN.
- (c.)Finally, the UPFC is install at the weak busses and the comparative analysis of voltage stability in terms of voltage profile, real and reactive power losses are measured and listed in terms of graphical and tabular results in order to validate the effectiveness of the present study.

## **1.2 Research aim and objective**

There are three main problems facing the design and implementing of FACTS devices:

- During the variable operating conditions and disturbance, the DC link capacitor voltage might collapse that will result the UPFC unable to control the power flow through power network.
- In real time operation, in different UPFC and its performance, there is a general lack of experimental validation
- The steady state analysis is not suitable for the wide range of operating conditions in the power system networks.

The main aim of this project is to improve the voltage stability in distribution network with the help of the UPFC controller to control the power flow of the network. This will result in

reduction of power losses and therefor it improves the power transfer capability. This includes:

- To model the power system network using IEEE-15 bus standard system with data sheet of system specifications using MATLAB software.
- To find the optimal location of FACTS by using voltage stability indices.
- Analysis of IEEE standard systems and to report for improvement in voltage profile with and without considering FACTS.

Respectively, the questions to be answered by thE proposed work are:

- (a) What is the accurate value of losses prevailing in the distribution network?
- (b) What is the influence of UPFC controller on distribution network instability and losses?

### **1.3 Problem statement**

In modern life, we have continuous advancements and hence the power demands keep increasing every day. Consequently, the power system network facing many problems such as voltage and frequency instability, power line overloaded and power system blackout. To meet these increasing power demands, one of the best solution is to construct a new power plant with new and advanced transmission as well as distribution system. However, it is very difficult to design and install new transmission as well as distribution system with advanced power system equipment's due to cost considerations, limited energy resources as well as due to environmental constrains. The creative solution is to enhance the existing power network by integrating advance power electronic devices such as FACTS devices in order to improve the power system quality, power system losses also to upsurge the power transfer capability from the utility to end users/ consumers.

### **1.4 Voltage stability**

Voltage stability: is defined the ability of a system to maintain voltage so that when load admittance is increased, load power will increase, and so that both power and voltage controllable [9]. Voltage stability generally spoken to by P-V and P-Q curves which is

appropriate strategy for showing the voltage instability phenomenon. In Fig. 1.1 below, different P-V curves are shown. A constant power factor, each curve has been assumed as  $Q = P \cdot \tan \phi$ .

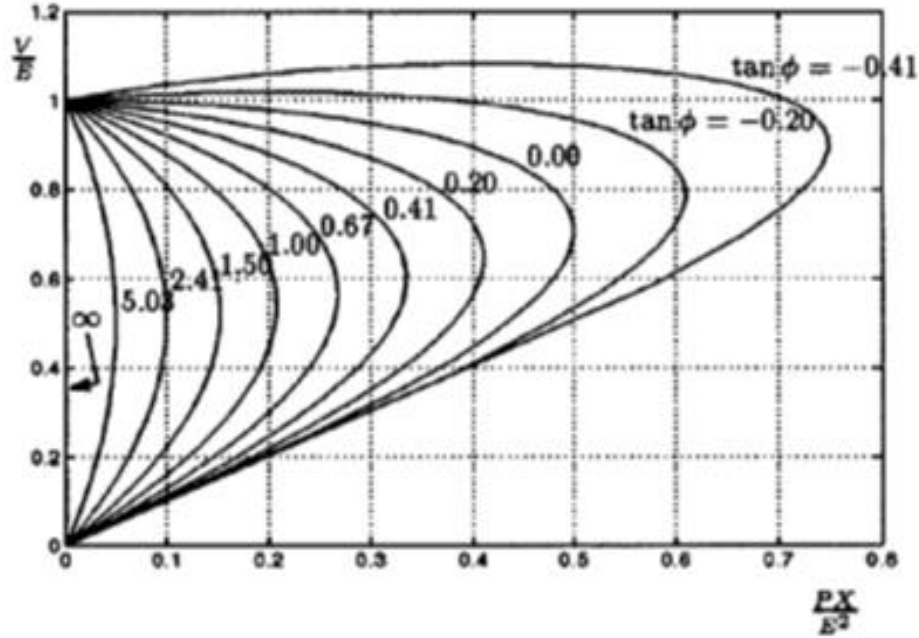


Figure 1.1: P-V Curve [12]

Frequently, The Q-V curves are an increasingly useful function for particular parts of the voltage stability studies. These can be utilized for assessing the necessities for the benefit of the reactive power since they show the affectability and variety of bus voltages regards to reactive power injections.

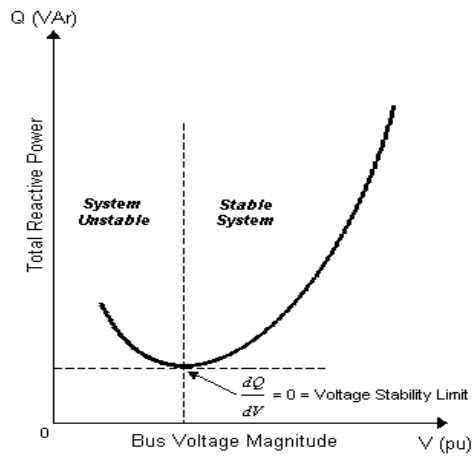


Figure 1.2: Q-V Curve [12]

Fig. 1.2 above, Shows a close Q-V curve to the P-V curves, Q-V curves consisting of the voltage stability limit, which is the fundamental part of the curve, where  $\frac{dQ}{dV}$  is equal to zero. The mechanism is stable on the right hand side, as an increase in Q is followed by an increase in voltage (V). The mechanism is unstable on the left hand side, since an increase in Q indicates a decrease in voltage (V). That judges that a system is unstable in voltage if the system has at least one bus, the magnitude of bus voltage decreases as the injection of reactive power in the same bus increases. In Fig. 1.3 presented below, the "nose curve" tip is known as the optimum loading point or critical point. Functioning close to the stability limit is impractical and the power margin is adequate, that is distance to the limit has to be allowed [13].

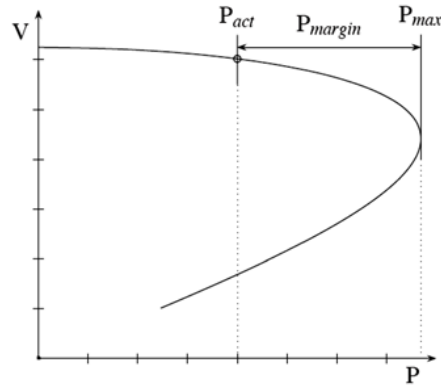


Figure 1.3: Power margin [12]

#### 1.4.1 Classification of voltage stability

In power system, the voltage instability occurs due to inability of power system to supply load centres under disturbances. As it shown in Fig. 1.4 below that in disturbances may be either large or small. Accordingly, voltage stability can be classified in following two subcategories:

- *Large-disturbance voltage stability* refers to the system's ability to maintain steady voltages following large disturbances such as system faults, loss of generation, or circuit contingencies. Determination of large disturbance voltage stability requires the analysis of non-linear response of power system. The study period of interest may extend from a few seconds to tens of minutes.

- *Small- disturbance voltage stability* refers to the system ability to maintain steady voltage under small disturbances such as incremental change in system load. With appropriate assumptions, system equations can be linearized for analysis. The time frame of interest for voltage stability problem may vary from a few seconds to tens of minutes. Therefore, voltage stability may be either short-term or long-term phenomenon.
- *Short-term voltage stability* Includes a strong phenomenon dynamics with a time-frame of fractions of a second to a few seconds. Operating load modules such as Automatic Voltage Regulator ( AVR) and electronic power converters such as Flexible AC Transmission System (FACTS) or High Voltage DC (HVDC) links. The analysis requires a solution of appropriate system differential equations [13].
- *Long-term voltage stability* involves dynamics of slower acting equipments such as tap-changing transformers, thermostatically controlled loads and generator current limiters. The study period of interest may extend to several or many minutes and long-term simulations are required for analysis of system dynamic performance [14-15].

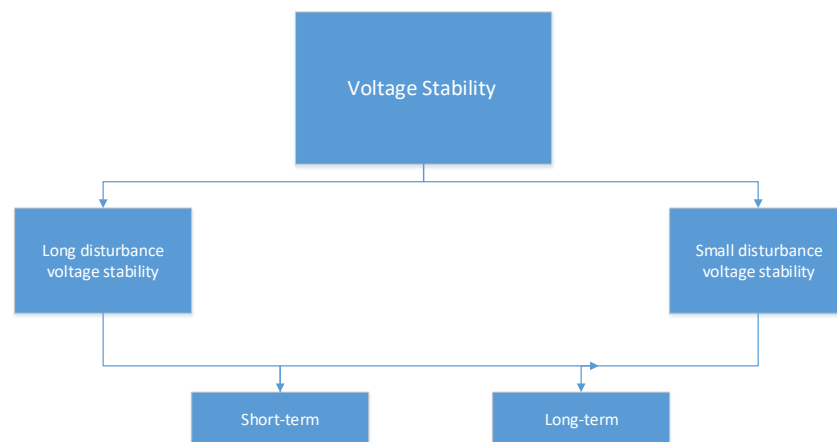


Figure 1.4: Classification of Voltage Stability

#### 1.4.2 Main cause of voltage stability problem

Some of the causes for occurrence of voltage instability are;

- Different in transmission of reactive power under heavy loads.

- High reactive power consumption due to heavy loads.
- Occurrence of contingencies.
- Voltage sources are too far from load centres.
- Due to unsuitable locations of FACTS controllers.
- Poor coordination between multiple FACTS controllers.
- Presence of constant power loads.
- Reverse operation of ON Load Tap-Changer (OLTC).

## 1.5 Scope

This research work will be based on modelling and simulation of an IEEE 15-bus test system (distribution feeder network) using *MATLAB/Simulink®*, to investigate and analyse a power distribution network with and without a Flexible Alternating Current Transmission Systems (FACTS) devices i.e. UPFC for reactive power compensation and voltage control. The optimal location of UPFC was carried out using two voltage stability indices namely: Line Stability Factor (LPQ) and Performance Index (PI). The results of simulations will then be studied which may involve statistical analysis, quantitative evaluation of network and other graphical interpretations of the various simulations.

## 1.6 Thesis organization

### ***Chapter 1: Introduction:***

This chapter will provide the introduction, background, problem statement, voltage stability and objectives.

### ***Chapter 2: Literature review:***

This chapter will review the research that has been undertaken in the topic area and provide analysis of the relevant material.

### ***Chapter 3: Research methodology:***

This chapter will focus on Voltage Stability Indices (VSI), their organisation, a presentation of each group and a comparison between them.

***Chapter 4: Simulation and Analysis:***

This chapter includes design, mathematical calculations, computer simulations and analysis of location as well as improvement in voltage profile in the distribution network.

***Chapter 5: Placement of UPFC in Distribution Network:***

This chapter present the identification as well as installation of UPFC in distribution network as well as results with improvement in voltage profile of the distribution network.

***Chapter 6: Conclusion:***

This chapter will provide general conclusion and recommendations which provides a scope for future research work.

## CHAPTER TWO

### LITERATURE REVIEW

#### 2.1 Power system overview

The power system network is a large interconnected system with different components connected with the main interest of supplying electric power to consumers. Usually a power system is divided into three system stages such as: generation, transmission, and distribution. Power generation is a site where the process of supplying power begins by converting energy that is available from the nature (wind, water, and sun) into electrical energy. Since generation is connected to the transmission lines, then the transfer via transmission system to the distribution system. Distribution stage is making the final conveyance of electrical power to customers. On the transmission is where the power losses occur because of the resistance ( $R$ ) and reactance ( $X$ ) of the line over a long distance, hence why on the distribution stage receiving 85% of the generated capacity by the generator, while the load is increasing every day, that results voltage instability in the distribution stage. Fig. 2.1 below, shows a typical power system network.

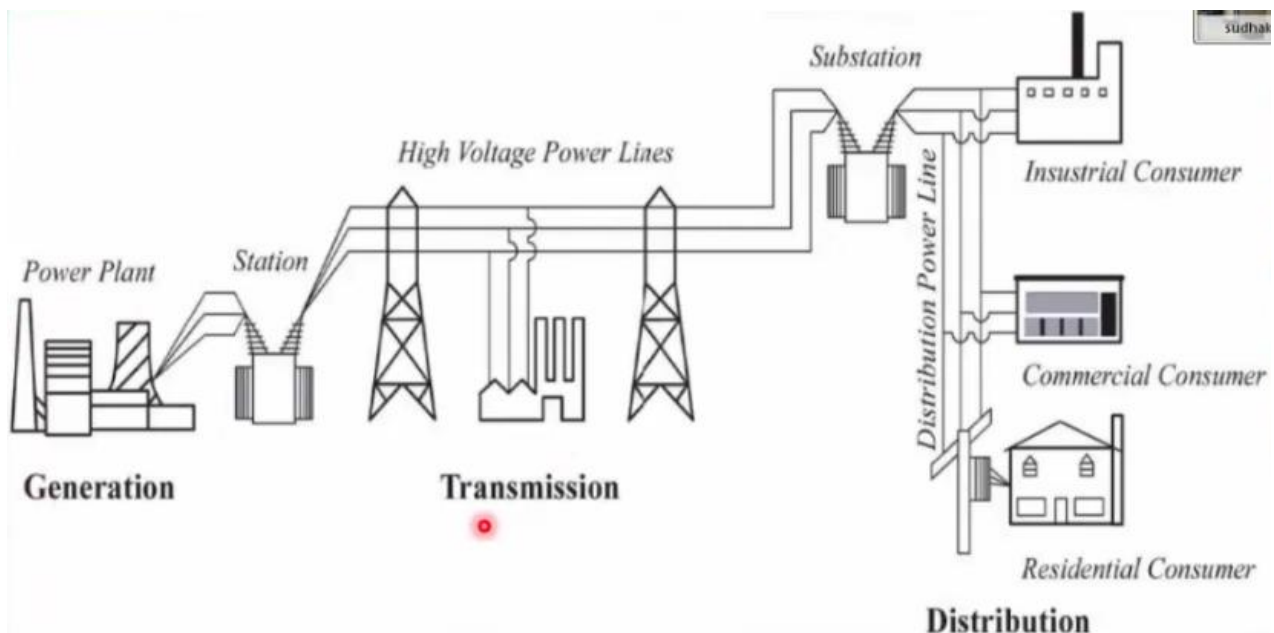


Figure 2.1: Power system network [16]



In 1991, GyuGyi propose The idea of UPFC, he was counselled for dynamic compensation and real time control of an alternating current transmission systems. In order to keep the voltage and current stable in the existing distribution network, permanent installation of FACTS devices should be done. The Thyristor Controlled Phase Shifting Transformer (TCPST) and by combining a shunt and series devices, UPFC is formed [17-18]. In a series compensation, the FACTS works as a controllable voltage source when connected in series with the power system [19]. In shunt compensation, the FACTS device is connected in shunt with the power system working as a controllable current source  $I_{sh}$  to control the line current  $I_L$ , as per ohm's law,  $V_s - V_R$  being the voltage drop across the transmission line correlate to the current flowing through the line. Considering the value of the sending end voltage ( $V_s$ ) to be fixed, the shunt device can easily control the magnitude of a receiving end voltage ( $V_R$ ) [20]. Series inductance happens in a long transmission line, and when an enormous current flowing through, it causes a huge voltage drops in the network [21-22].

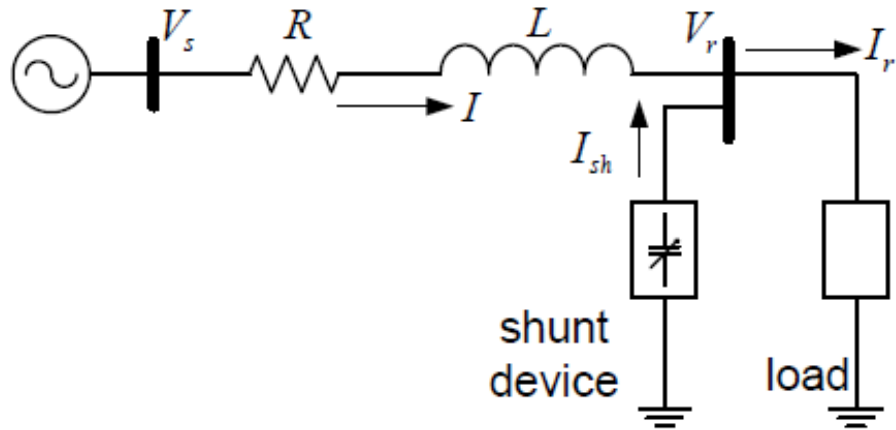


Figure 2.2: Shunt device operating mechanism [20]

The equation below predicts the link between the injected current  $I_{sh}$  by the shunt device and the voltage at receiving end:

$$V_R = (V_s - I \cdot Z) \dots\dots\dots (2.1)$$

Therefore

$$V_S = V_R - (I_R - I_{Sh}) \cdot Z \dots\dots\dots(2.2)$$

Where:

$$Z = R + j\omega L \dots\dots\dots(2.3)$$

$$V_{Reg} = \frac{V_S - V_R}{V_R} \cdot 100\% \dots\dots\dots(2.4)$$

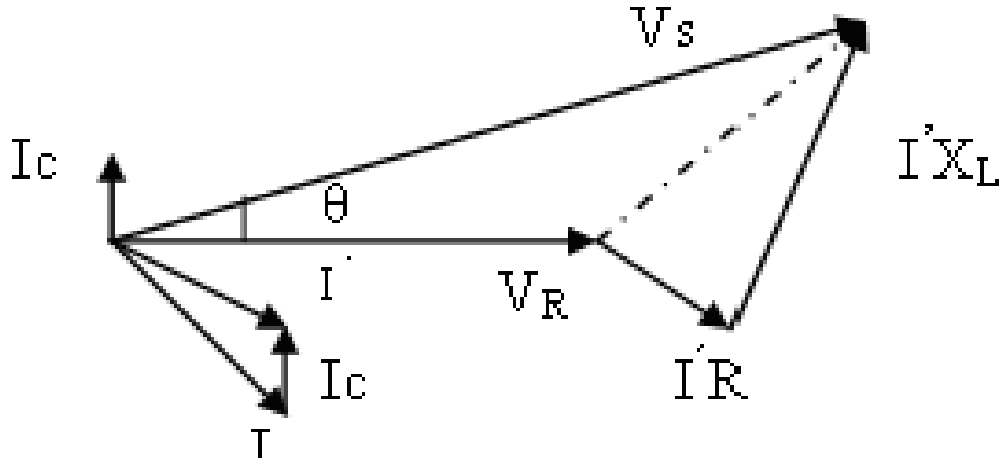


Figure 2.3: Voltage-phasor diagrams for a feeder circuit with shunt [23]

## 2.2 FACTS devices

### 2.2.1 Introduction

The endeavour of FACTS devices is very effective and capable in terms of power transfer incremental of the distribution network, as thermal limits permit, while same angle of stability is maintained [24]. For long-term solutions many recent applications of FACTS have proven to be lucrative. In voltage and current enhancements managing capabilities of the power electronic devices that have permitted the FACTS device in development, the opportunities in using different types of controllers for effective shunt and series compensation has arisen [25]. Series and shunt FACTS devices, on a broad-scale basis, are useful for computing and analysing a transmission voltage, power flow, mitigation of

reactive losses and power system oscillations damping for high power transfer levels [26-27]. Shunt capacitive compensation is useful in power factor correction. When the inductive load is connected to the power network, the power factor is lagging the potential difference by 90 degrees caused by the lagging load current. In [28-29] shunt capacitor is connected to results current leading the voltage from the source ( $V_s$ ). Fig. 2.4 shows the general classification of FACTS devices done on their basis of their types of arrangement in the network.

*Table 2.1: Shows the FACTS family*

| Type         | Thyristor-controlled |       |        |        | Converter-based |        |      |        |
|--------------|----------------------|-------|--------|--------|-----------------|--------|------|--------|
|              | SVC                  |       | TCSC   | TCPAR  | STATCOM         | SSSC   | UPFC | IPFC   |
|              | TSC                  | TCR   |        |        |                 |        |      |        |
| Compensation | Shunt                | Shunt | Series | Series | Shunt           | Series | Both | Series |

*Table 2.2: Cost comparison of various FACTS devices*

| Compensation device | Cost                       |
|---------------------|----------------------------|
| SVC                 | 40 KVAR Controlled portion |
| TCSC                | 40 KVAR Controlled portion |
| STATCOM             | 50 KVAR                    |
| UPFC                | 50 KVAR Through power      |
| IPFC                | 50 KVAR Controlled portion |

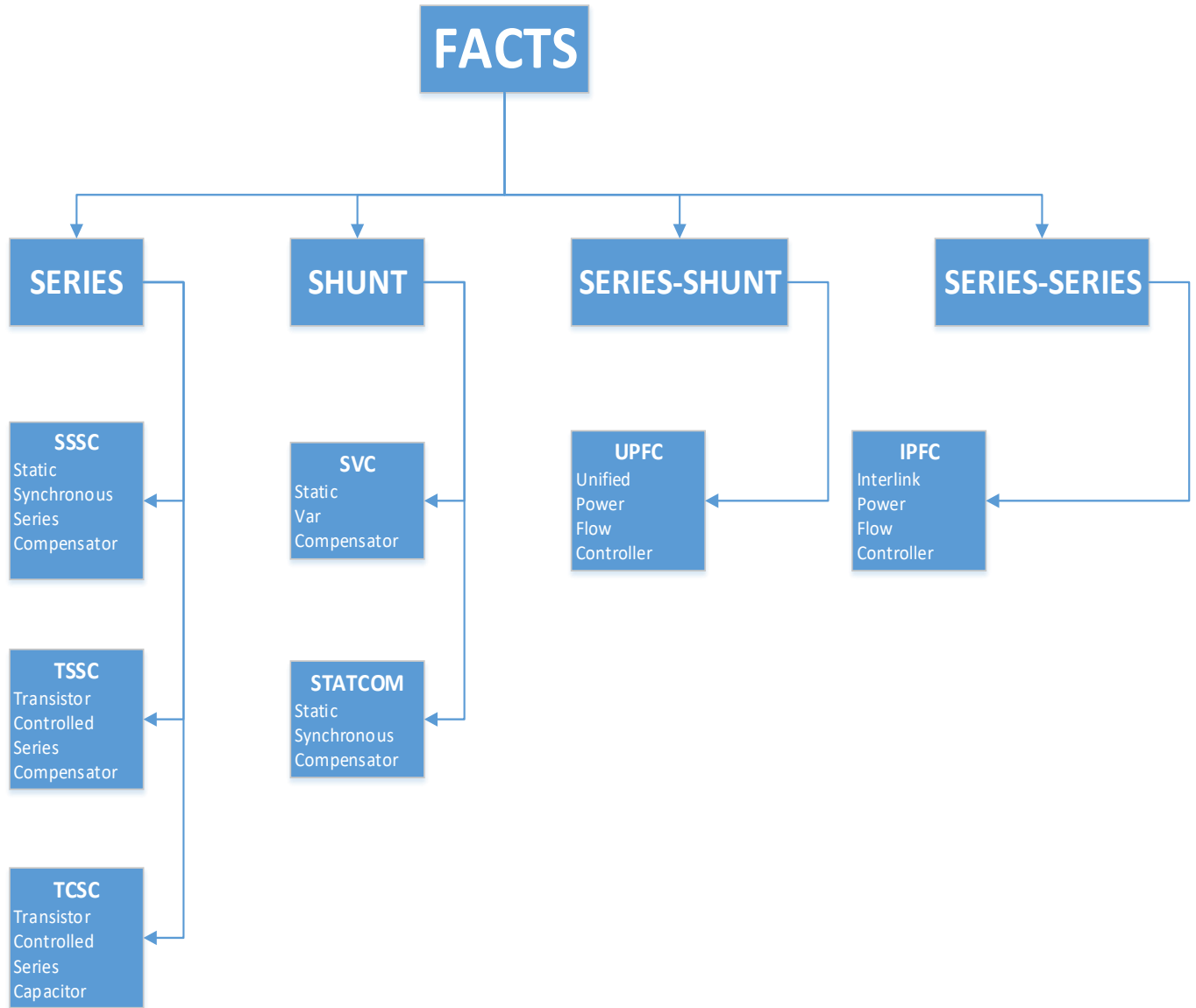


Figure 2.4: Classification of FACTS devices

Fig. 2.5 demonstrate some typical configurations of Voltage Source Converters (VSC)-based FACTS devices. controllers provide the series, shunt or combination of series and shunt compensation to the system by injecting a series voltage or shunt current into the connected line via a series or shunt voltage-sourced switching converter. Combining shunt and series compensation can provide comprehensive compensation to the system. In [30], this group of FACTS devices includes the Static Synchronous Compensator (STATCOM), the Static Synchronous Series Compensator (SSSC), the Unified Power Flow Controller (UPFC) and the Interline Power Flow Controller (IPFC). The STATCOM,

like the SVC, provides shunt compensation to the system by controlling the reactive current injected into the shunt-connected line thereby affecting the voltage

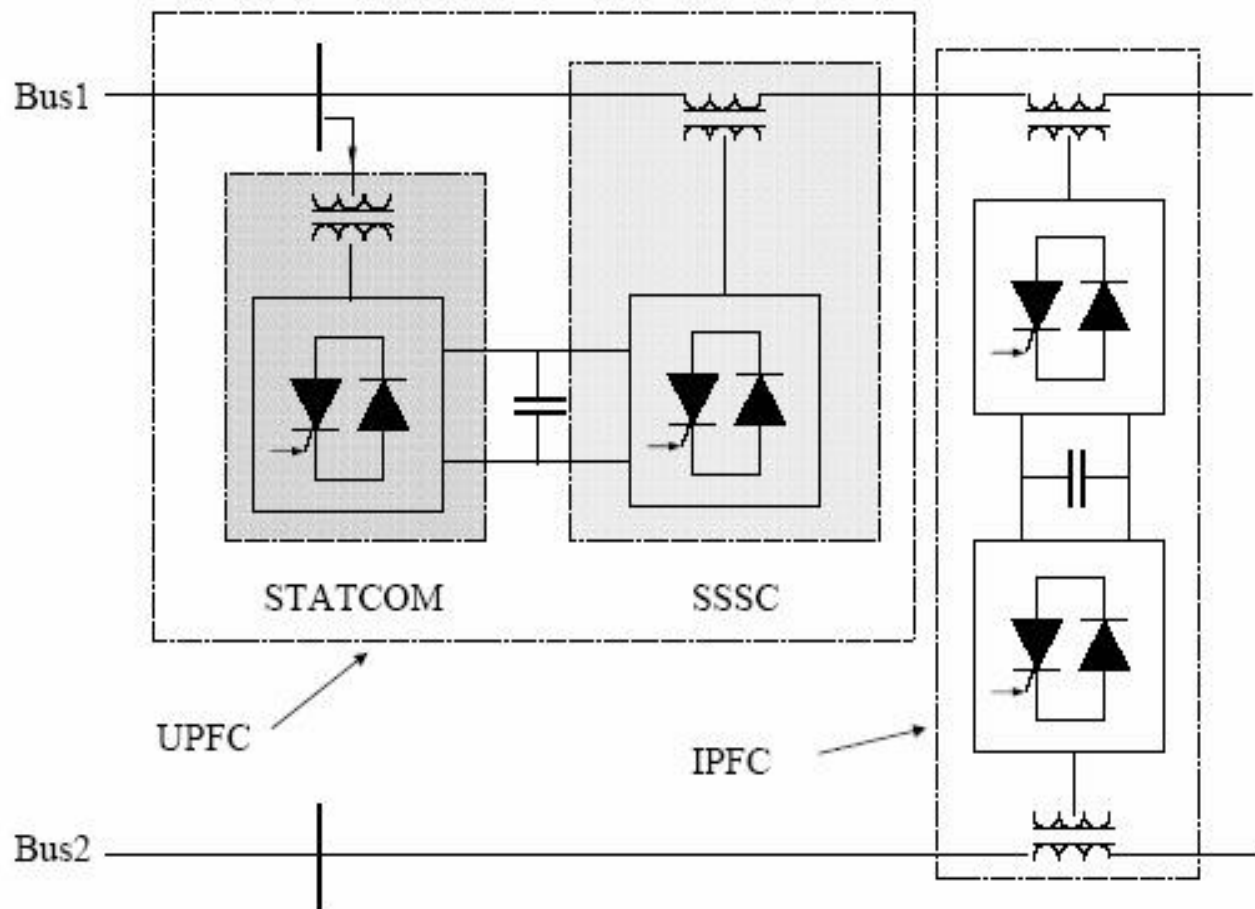


Figure 2.5: Voltage Source Converters based FACTS [30]

## 2.2.2 Static Synchronous Series Compensator (SSSC)

### 2.2.2.1 Overview of an SSSC

An SSSC is one of the devices in the FACTS family that is permanently installed in-series with the line, the SSSC utilizing a voltage source converter to infuse a controllable voltage is quadrature with the line current of a power system can quickly give both capacitive and inductive impedance compensation independent of the power line current [31]. These highlights make the SSSC an appealing FACTS device for control of power flow, power oscillation damping and transient stability improvement.

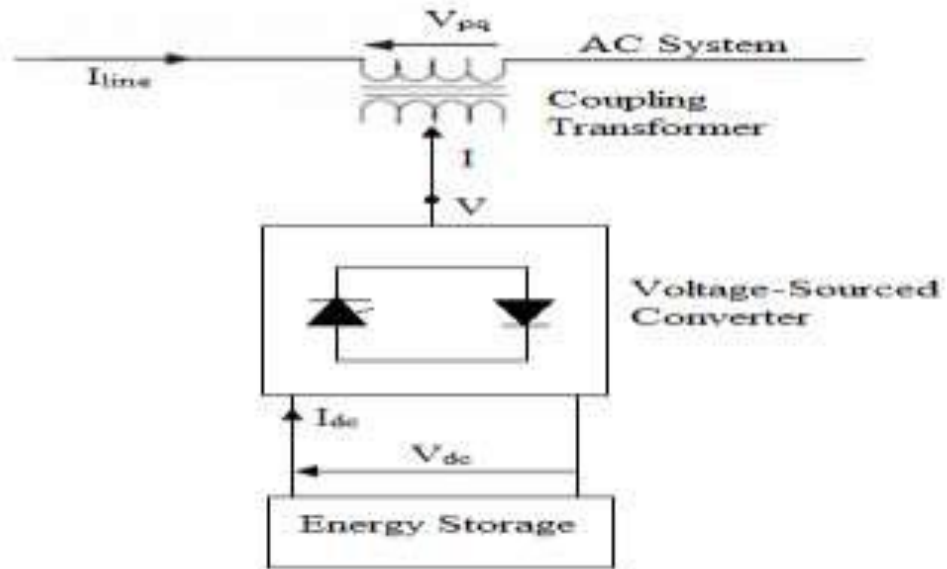


Figure 2.6: Functional model of SSSC [32]

### 2.2.2.2 Principle of operation of an SSSC

The Static Synchronous Series Compensator is made up of three basic components namely:

- *Voltage Source Converter (VSC)* – main component
- *Transformer* – couples the SSSC to the distribution network
- *Energy Source* – provides voltage across the DC capacitor.

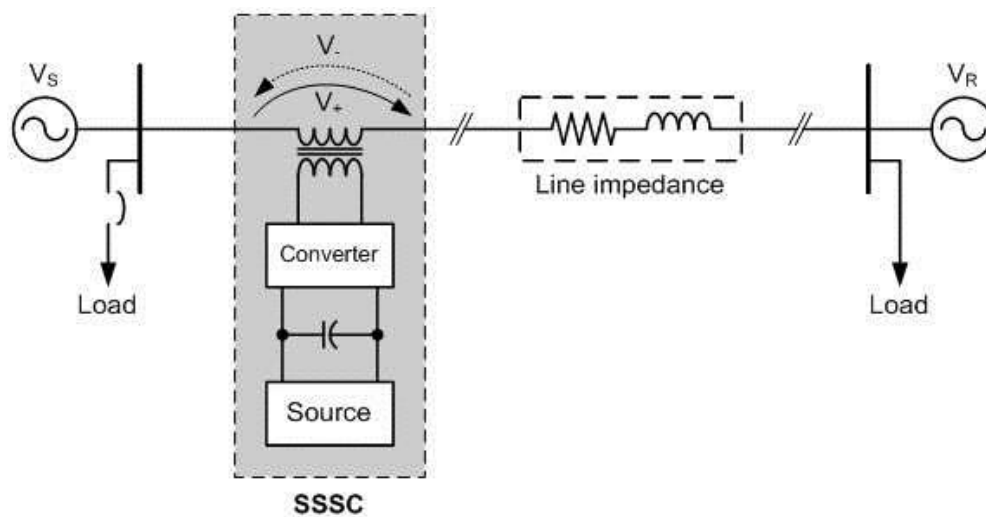


Figure 2.7: Static Synchronous Series Compensator (SSSC) Diagram [31]

The SSSC is typically connected in series with the distribution feeder with the arrangement as appeared in Fig. 2.7. The SSSC includes a DC capacitor, coupling transformer with magnetic interface, and the voltage source converters (VSC). The coupling transformer is connected in series with the distribution feeder and it injects the quadrature voltage into the distribution feeder. As harmonics are available, then the magnetic interface eliminate those harmonics by providing multi-pulse voltage configuration. The injected voltage of the coupling transformer  $V_{pq}$  is perpendicular to the line current  $I_L$ . The SSSC's output voltage magnitude and phase angle can be varied in a controlled manner to influence power flows in a distribution feeder. The phase displacement of the inserted voltage  $V_{pq}$ , with respect to the distribution feeder current line  $I_L$  controls the exchange of active and reactive power with the AC system.

### 2.2.2.3 Mode of operation of an SSSC

Usually the line reactance is constant but its net effect can be controlled through voltage injection as its depicted in Fig. 2.8. As, the line current decreases as the inductive reactance compensation level increases from 0% to 100%. Temporarily, the increment in capacitive reactance compensation level from 0% to 33%, the line current would then increase.

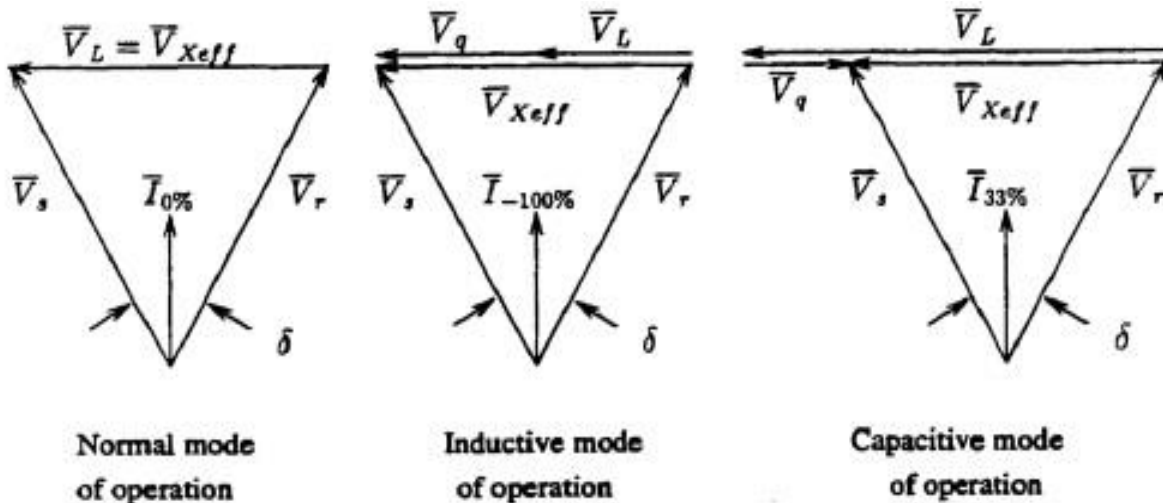


Figure 2.8: Mode of operation of SSSC [33]

It can be noted that the static synchronous series compensator does not only increase the transferable power but it can also decrease it, by simply swapping the polarity of the vaccinated voltage. This reversed polarity voltage is fed directly to the line voltage drop as if the line impedance was increased [33].

#### 2.2.2.4 SSSC power flow equations

Refer to Fig. 2.7, the active and reactive power flow (P and Q) at the receiving end is given by:

$$P = \frac{V_s \cdot V_R}{X_L} \sin(\delta_s - \delta_R) \dots\dots\dots(2.5)$$

For the simplicity, the voltage magnitudes are taken constant that is,

$$V_s = V_R = V \dots\dots\dots(2.6)$$

Therefore

$$P = \frac{V^2}{X_L} \sin\delta \dots\dots\dots(2.7)$$

$$Q = \frac{V_s \cdot V_R}{X_L} (1 - \cos(\delta_s - \delta_R)) \dots\dots\dots(2.8)$$

Therefore

$$Q = \frac{V^2}{X_L} (1 - \cos\delta) \dots\dots\dots(2.9)$$

For reactive power compensation  $X_q$ , capacitive and inductive, the equation (2.7) and (2.9) can be expanded as;



$$P_q = \frac{V^2}{X_{Ref}} \sin\delta = \frac{V^2}{X_L \left(1 - \frac{X_q}{X_L}\right)} \sin\delta \dots\dots\dots(2.10)$$

$$Q_q = \frac{V^2}{X_{Ref}} (1 - \cos\delta) = \frac{V^2}{X_L \left(1 - \frac{X_q}{X_L}\right)} (1 - \cos\delta) \dots\dots\dots(2.11)$$

where, effective reactance of the distribution feeder including variable resistance embedded by the injected voltage source of SSSC. The compensating reactance  $X_q$  will be negative when the Series Compensator is operated in an inductive mode and will be positive when the Series Compensator is operated in a capacitive mode [34].

## 2.2.3 Static Synchronous Compensator (STATCOM)

### 2.2.3.1 Overview of a STATCOM

The mainstream of power consumption has been drawn in inductive loads especially industrials, they operate at a lagging power factor because reactive power  $Q$  is high. This result power losses and distribution system instability. The Static Synchronous Compensator (STATCOM) is one of the FACTS devices that is usually connected in shunt with the distribution feeder for voltage stability improvement and reactive power compensation.

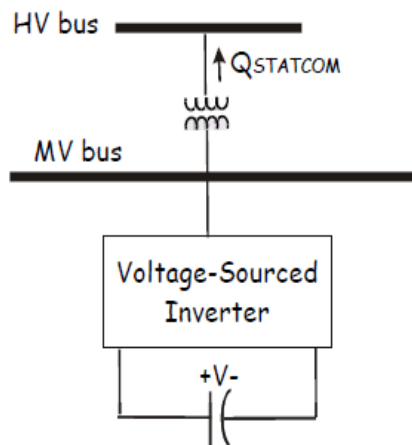


Figure 2.9: Configuration of STATCOM [35]

Fig. 2.9 depict STATCOM installed in the distribution network, from the DC capacitor; it generates a three-phase voltage in sync with the grid voltage via a coupling transformer, it improves the static and dynamic voltage stability of bus on power network, and keeps the voltage of the electric system in receivable operating mode [36]. The injected AC current of this device is either leading or lagging with grid voltage and it acts as an inductive and capacitive impedance at the point of connection [38]. If the voltage generated by the STATCOM is lesser than the grid voltage, it will emulate an inductive load and withdraw reactive power from the system. Also, when the device voltage is higher than the grid voltage, it would then match a capacitive load and provide reactive power to the distribution feeder [39].

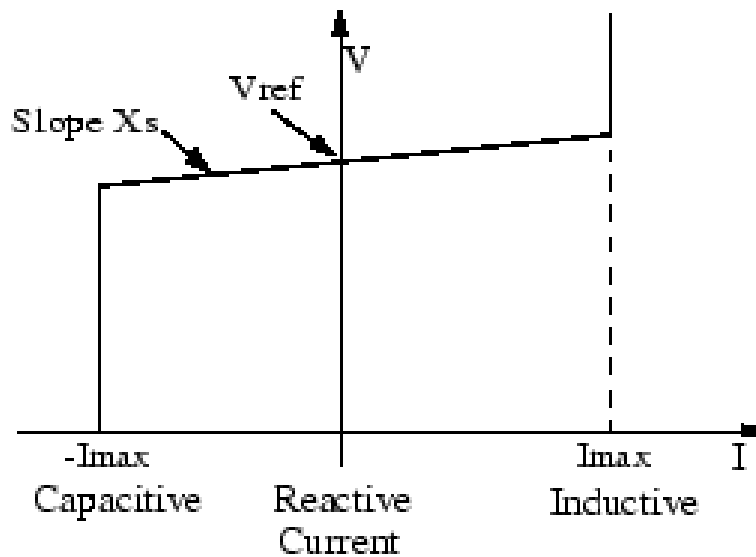


Figure 2.10: Terminal characteristic of STATCOM [37]

### 2.2.3.2 D-STATCOM and E-STATCOM

A Distribution Static Synchronous Comparator (D-STATCOM) is a shunt connected device as depicted in Fig. 2.11, as the alteration of a normal STATCOM used in the distribution system that injects reactive power into the system and controlling of voltage during transient events, voltage drops, eliminate harmonic level of current, load balancing and stability.

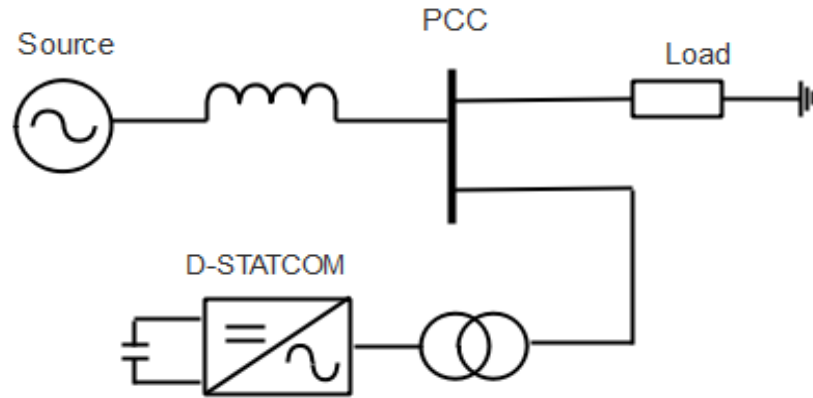


Figure 2.11: Shows a D-STATCOM on a distribution system [40]

While Energy Storage Static Synchronous Compensator (E-STATCOM) has a similar use to D-STATCOM, with the exclusion of its energy storing capacity that use to exchanges active power with the system. Fig. 2.12 shows the E-STATCOM.

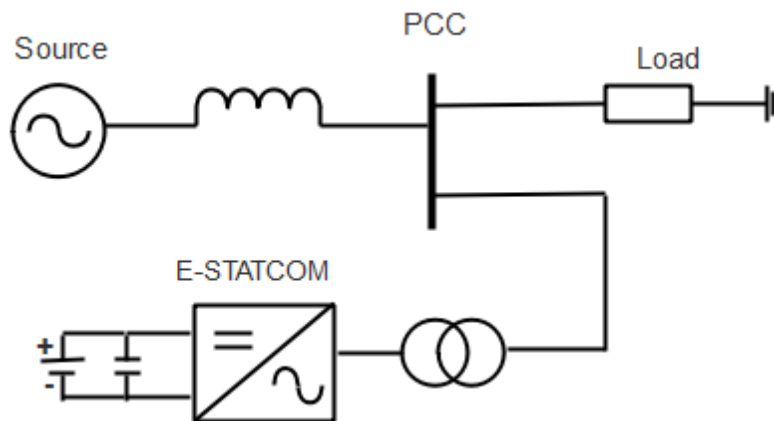


Figure 2.12: E-STATCOM on a distribution system [41]

## 2.2.4 Unified Power Flow Controller (UPFC)

### 2.2.4.1 Overview of a UPFC

The advance power electronic device that is capable in controlling the power flow in a network without making any rescheduling in a power generation. A UPFC is a solid-state multi-functional FACTS controller with the aptitude to control three parameters that influence the power flow such as: bus voltage magnitude, phase angle between two buses and line reactance, either concurrently or independently. UPFC can control not only for controlling the power flow, but also for power system stabilizing control.

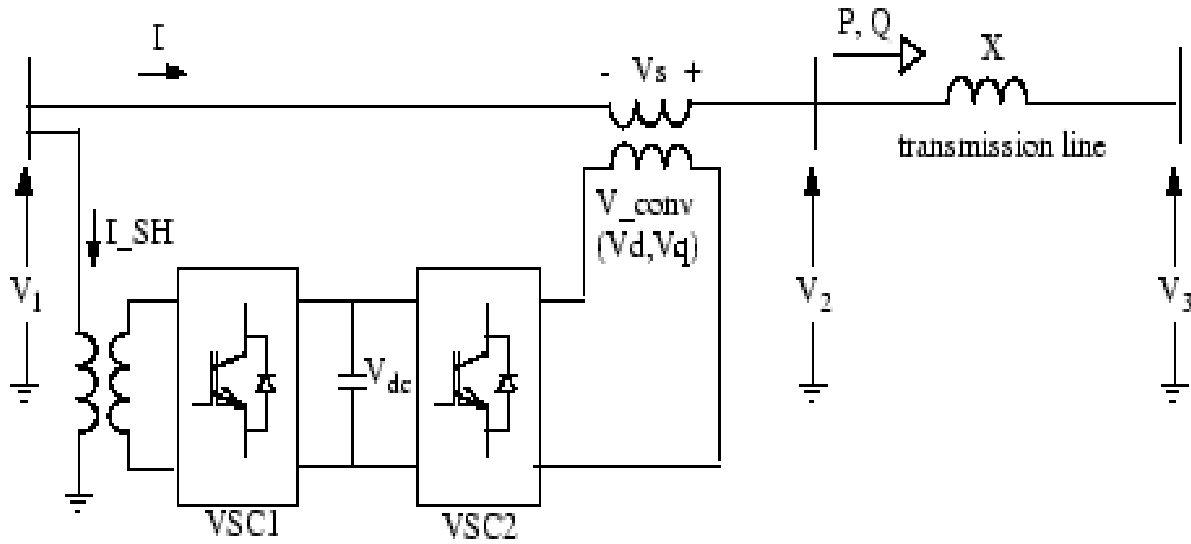


Figure 2.13: UPFC arrangement configuration [42]

As presented in Fig. 2.13 above, the UPFC containing two Voltage Source converters (VSC1) and (VSC2) which is shunt and series converters. The shunt converter is connected with distribution feeder in parallel through shunt transformer, while series converter is connected with distribution feeder in series through series transformer. These transformers are employed to provide the isolation between the power converters and the power system and to step the voltage level down from the bus voltage to the required voltage of the UPFC capacity. From the power network, the active and reactive (P-Q) power exchange between voltage source converter and the grid system occur as the line current flows through VSC. active power can now be transferred from the shunt converter to the series converter, through the DC bus. In [43], contrary to the SSSC where the injected voltage  $V_s$  is constrained to stay in quadrature with line current  $I$ , the injected voltage  $V_s$  can now have any angle with respect to line current.

#### 2.2.4.2 Equivalent circuit and power flow equations of a UPFC

In order to evaluate the impact of UPFC in the system network, formulation based on the circuit arrangement is essential, the equivalent circuit of UPFC is shown in Fig. 2.14 below, as injected shunt voltage  $V_{Sh}$  and series voltage source  $V_{Se}$  are representing the equivalent.  $Z_{Sh}$  and  $Z_{Se}$  are coupled with UPFC transformers impedances,  $V_k$  and  $V_m$

are bus to bus voltages or sending and receiving end voltage. Series and shunt voltages can be written as:

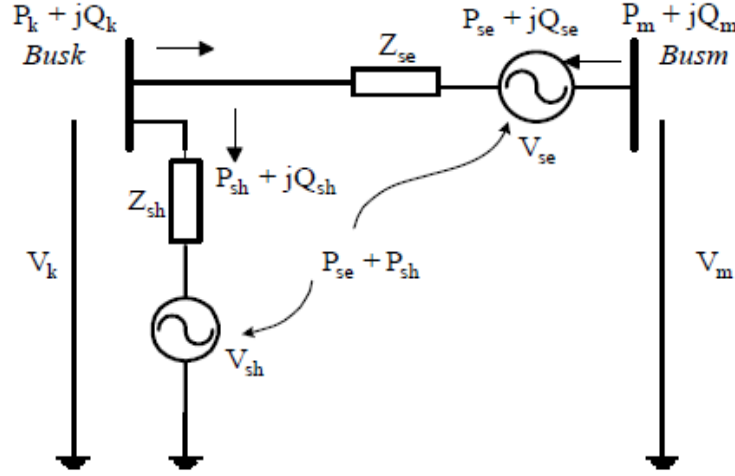


Figure 2.14: Equivalent circuit of UPFC [43]

$$V_{se} = V_{se} (\cos \theta_{se} + j \sin \theta_{se}) \dots\dots\dots (2.12)$$

$$V_{sh} = V_{sh} (\cos \theta_{sh} + j \sin \theta_{sh}) \dots\dots\dots (2.13)$$

Then UPFC active power and reactive power equation can be written as follows:

@ node  $k$

$$\begin{aligned} P_k &= V_k^2 G_{kk} + V_k V_m (G_{km} \cos(\theta_k - \theta_m) + B_{km} \sin(\theta_k - \theta_m)) \\ &+ V_k V_{se} (G_{km} \cos(\theta_k - \theta_{se}) + B_{km} \sin(\theta_k - \theta_{se})) \dots\dots\dots (2.14) \\ &+ V_k V_{sh} (G_{sh} \cos(\theta_k - \theta_{sh}) + B_{sh} \sin(\theta_k - \theta_{sh})) \end{aligned}$$

$$\begin{aligned} Q_k &= -V_k^2 B_{kk} + V_k V_m (G_{km} \sin(\theta_k - \theta_m) - B_{km} \cos(\theta_k - \theta_m)) \\ &+ V_k V_{se} (G_{km} \sin(\theta_k - \theta_{se}) - B_{km} \cos(\theta_k - \theta_{se})) \dots\dots\dots (2.15) \\ &+ V_k V_{sh} (G_{sh} \sin(\theta_k - \theta_{sh}) - B_{sh} \cos(\theta_k - \theta_{sh})) \end{aligned}$$

@ node  $m$

$$\begin{aligned} P_m &= V_m^2 G_{mm} + V_m V_k (G_{mk} \cos(\theta_m - \theta_k) + B_{mk} \sin(\theta_m - \theta_k)) \dots\dots\dots (2.16) \\ &+ V_m V_{se} (G_{mm} \cos(\theta_m - \theta_{se}) + B_{mm} \sin(\theta_m - \theta_{se})) \end{aligned}$$

$$Q_m = -V_m^2 B_{mm} + V_m V_k (G_{mk} \sin(\theta_m - \theta_k) - B_{mk} \cos(\theta_m - \theta_k)) + V_m V_{sh} (G_{mm} \sin(\theta_m - \theta_{se}) - B_{mm} \cos(\theta_m - \theta_{se})) \dots (2.17)$$

Series converter:

$$P_{se} = V_{se}^2 G_{mm} + V_{se} V_k (G_{km} \cos(\theta_{se} - \theta_k) + B_{km} \sin(\theta_{se} - \theta_k)) + V_{se} V_m (G_{mm} \cos(\theta_{se} - \theta_k) + B_{mm} \sin(\theta_{se} - \theta_m)) \dots (2.18)$$

$$Q_{se} = -V_{se}^2 B_{mm} + V_{se} V_k (G_{km} \sin(\theta_{se} - \theta_k) - B_{km} \cos(\theta_{se} - \theta_k)) + V_{se} V_m (G_{mm} \sin(\theta_{se} - \theta_m) - B_{mm} \cos(\theta_{se} - \theta_m)) \dots (2.19)$$

Shunt converter:

$$P_{sh} = -V_{sh}^2 G_{sh} + V_{sh} V_k (G_{sh} \cos(\theta_{sh} - \theta_k) + B_{sh} \sin(\theta_{sh} - \theta_k)) \dots (2.20)$$

$$Q_{sh} = V_{sh}^2 B_{sh} + V_{sh} V_k (G_{sh} \sin(\theta_{sh} - \theta_k) - B_{sh} \cos(\theta_{sh} - \theta_k)) \dots (2.22)$$

Where

$$Y_{kk} = G_{kk} + jB_{kk} = Z_{se}^{-1} + Z_{sh}^{-1} \dots (2.23)$$

$$Y_{mm} = G_{mm} + jB_{mm} = Z_{se}^{-1} \dots (2.24)$$

$$Y_{sh} = G_{sh} + jB_{sh} = -Z_{sh}^{-1} \dots (2.25)$$

Assuming that during the operation the converter is lossless, therefore, the active power supplied to the shunt converter  $P_{sh}$  is equal to the active power the series converter  $P_{se}$  demands.

Then

$$P_{se} + P_{sh} = 0 \dots (2.26)$$

Also, if the coupling transformers resistances are negligible, so the active power in bus  $k$  is equal to that in bus  $m$  ; This can be represented as;

$$P_{sh} + P_{se} = P_k + P_m = 0 \dots\dots\dots(2.27)$$

The UPFC power equations are linearized and combined with the equations of the AC transmission network for the cases where UPFC controls parameters. Equation (2.27) described that the active power exchange between shunt and series converters via DC link is balanced at any instant.

### 2.2.4.3 Control strategy for a UPFC

In order for active power and reactive power to be controlled in the network, injection of series voltage is essential. Fig. 2.15 describe that line quantities such as: voltage and current can be transformed into d-q frame of reference at,  $t=0$  A-axis are in phase with q-axis. As UPFC consisting of two voltage source converters, therefore UPFC can control power and reactive power simultaneously or independently using series injected voltage. The shunt current would then have controlled by shunt converter voltage varieties. Shunt converter is accountable for AC bus voltage and DC-link voltage control.

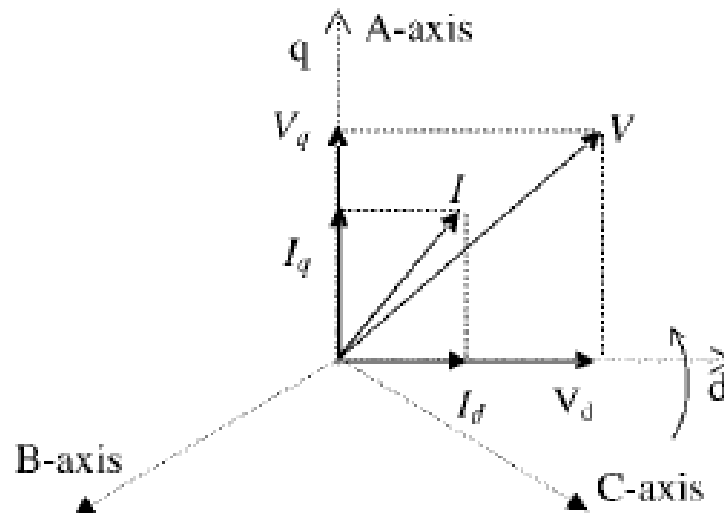


Figure 2.15: Definition of orthogonal co-ordinates [44]

## 2.2.5 Interlink power flow controller (IPFC)

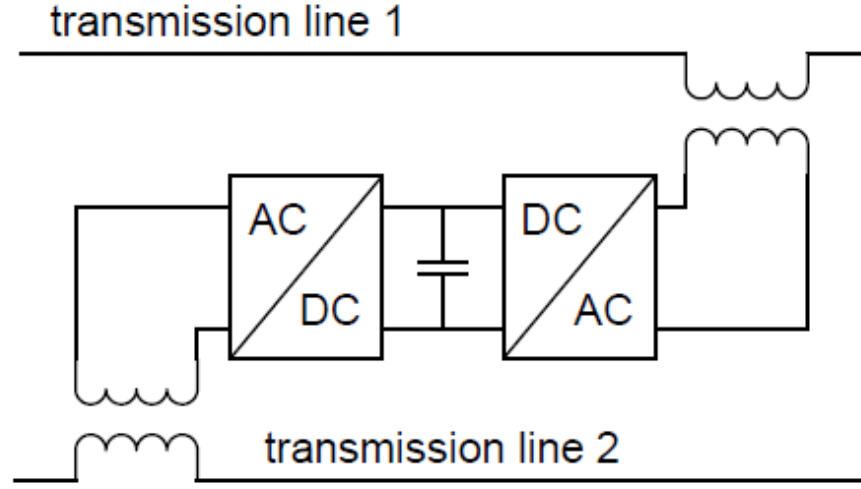


Figure 2.16: Interline Power Flow Controller configuration [45]

IPFC is a two SSSCs connected in-series of each line feeder to provide power flow control of the network. The IPFC consist of a back-to-back DC-to-AC converter each providing series reactive power compensation for different lines. The converters are connected together with their DC terminals, and connected to the AC systems through their series coupling transformers. Furthermore, any converter can be controlled by its own distribution feeder to supply active power to the common dc link [46]. Two separate SSSCs are placed at the weakest bus, IPFC has the following control attributes; RP control, Voltage control, Power Oscillations Damping, VS, TS and DS [47]. The controllable parameters of this device is the magnitude of the series voltage sources; The voltages sources are regulated by the respective PD controllers. The following equations of two SSSCs that making up the IPFC are:

SSSC 1

$$V_{S1} = (V_{S1}^0 + V_{S1}^{PD1} - V_{S1}) \cdot T_{r1} \dots\dots\dots (2.28)$$

$$V_{S1}^0 = K_{p1} (P_{ref1} - P_{km1}) + V_{pi1} \dots\dots\dots (2.29)$$

$$V_{pi} = K_{i1} (P_{ref1} - P_{km1}) \dots\dots\dots (2.30)$$



## SSSC 2

$$V_{S2} = (V_{S2}^0 + V_{S2}^{PD2} - V_{S2}) \cdot T_{r2} \dots\dots\dots (2.31)$$

$$V_{S2}^0 = K_{p2} (P_{ref2} - P_{kn2}) + V_{pi2} \dots\dots\dots (2.32)$$

$$V_{p2} = K_{i2} (P_{re2} - P_{kn2}) \dots\dots\dots (2.33)$$

### 2.2.5.1 Equivalent circuit of an IPFC

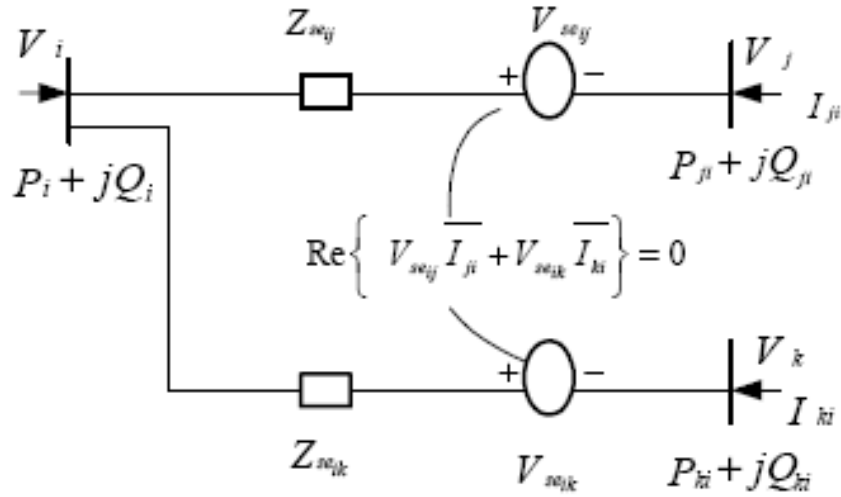


Figure 2.17: Equivalent circuit of IPFC [48]

For the system shown in Fig 2.17, the received power and the injected reactive power at the receiving end of the system line can be expressed as:

$$P_i = P_{ji} + \frac{V_{ji}}{X} \sin\left(\frac{\delta_j}{2} - \phi_j\right) + \frac{V_{ki}}{X} \cos\left(\frac{\delta_k}{2} - \phi_k\right) \dots\dots\dots (2.34)$$

$$Q_i = Q_{ji} + \frac{V_{ji}}{X} \cos\left(\frac{\delta_j}{2} - \phi_j\right) + \frac{V_{ki}}{X} \sin\left(\frac{\delta_k}{2} - \phi_k\right) \dots\dots\dots (2.35)$$

Where

$$\delta_i = \theta_i - \theta_k \sin \phi_i = \frac{V_{ji}}{2V \sin \frac{\delta}{2}} \dots\dots\dots (2.36)$$

Equation (2.34) and (2.35) are the active and reactive power for the distribution line.

## 2.3 Development of a Fuzzy Logic Controller (FLC) based UPFC

### 2.3.1 Overview

A Fuzzy Logic Controller (FLC) based UPFC is use to provide a better power flow control in the network under different operating conditions and it's also improve the power quality of the power network as expected by the customers. Efficiently, FLC has the capability to solve the complex system network problems. Furthermore, the FL controller is robust and can provide a dynamic power flow control under different operating conditions [49]. UPFC is the most multipurpose device compare to other FACTS devices. Fig. 2.18 shows arrangement of a Fuzzy Logic Controller (FLC) based UPFC dynamic model. UPFC is mainly consisting of shunt and series VSCs, where shunt VSC perform as STATCOM and series VSC perform as SSSC independently. The common DC link capacitor is used to link these converters. Both these converters are connected to the distribution feeder through two transformers in order to provide the isolation between power distribution and power converters. For switching purposes, both converters use Insulated Gate Bipolar Transistors (IGBTs) [50]. Low pass AC filters are designed to mitigate the harmonic due to switching events. FLC based UPFC is developed for both shunt and series converter as it depicted in Fig. 2.18. The controlling strategy for both converters is explained in the following section.

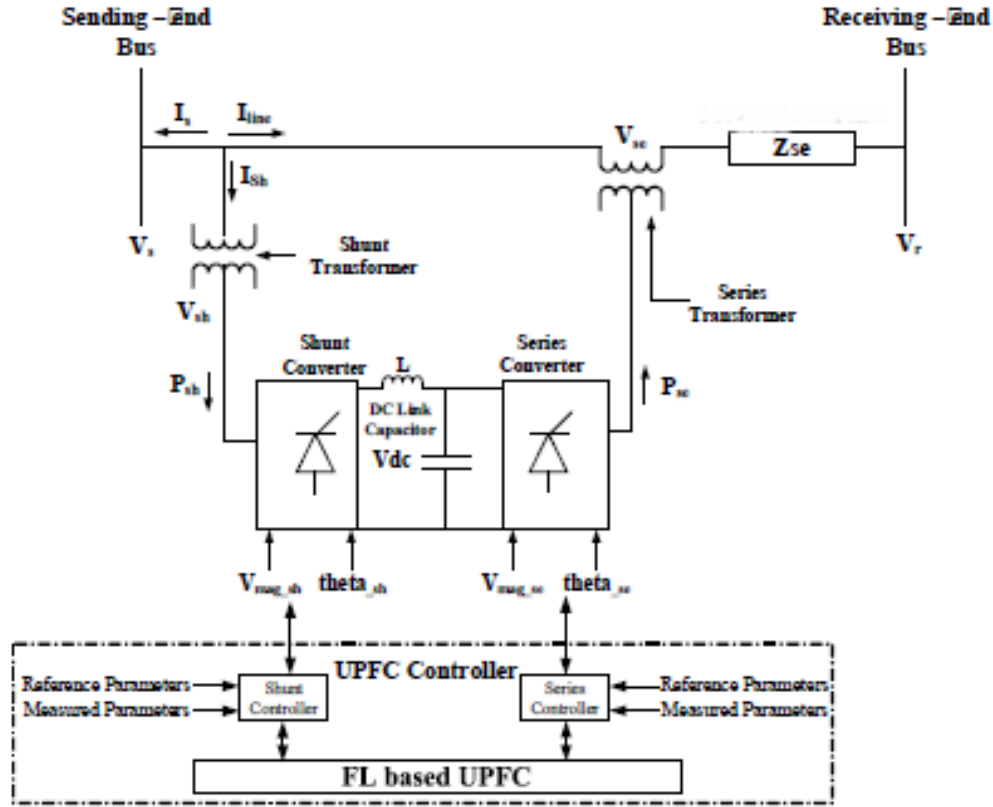


Figure 2.18: Arrangement of a Fuzzy Logic Controller (FLC) based UPFC [50]

### 2.3.2 Shunt controller of a UPFC based on FLC

The shunt converter of a FLC is used to produce  $(\alpha_{sh})$  and  $(V_{mag\_sh})$  by subtracting measured voltage of a DC link capacitor and sending in bus voltage to its reference values. See Fig. 2.19, the shunt converter is to maintain the voltage of the DC link capacitor and the sending in bus voltage by comparing them with their reference values and send to FLC. Basically in FLC there are two main outputs which is: error and error rate. As the output of the sending in bus voltage generate  $(V_{mag\_sh})$  and theta  $(\alpha_{sh})$  is generated by voltage of the DC link capacitor, will then compare with the sawtooth to produce the required Sinusoidal Pulse Width Modulation (SPWM) signal for shunt converter IGBTs, see Fig. 2.19. In any progressive connected application, the synchronisation is considered between the injected voltage magnitude  $(V_{mag\_sh})$  and theta  $(\alpha_{sh})$ , to ensure that synchronisation Phase Lock Loop (PLL) is essential. PLL is

employed to find the angle of the bus voltage and comparing by subtracting the angle from the DC link capacitor ( $\alpha_{sh}$ ) to produce the phase angle of the shunt reference of the sine wave.

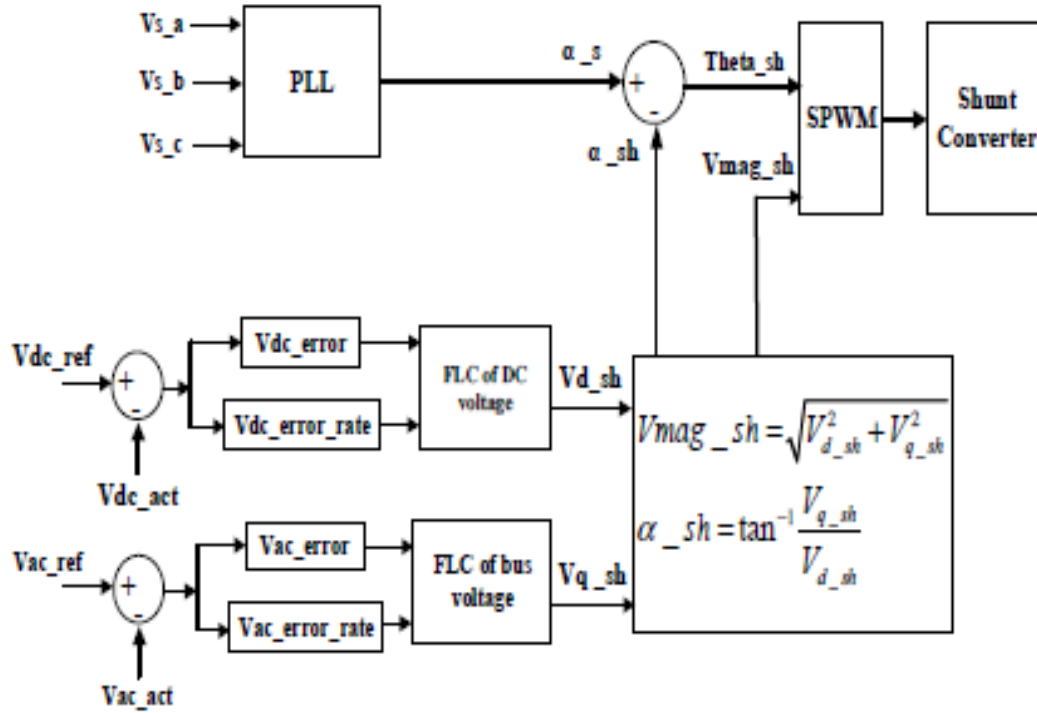


Figure 2.19: Shunt controller of sending-end voltage and DC link voltage to generate  $(V_{mag\_sh})$  and  $(\alpha_{sh})$  [51]

The generated voltage magnitude and theta is expressed as follows:

$$V_{mag\_sh} = \sqrt{V_{d\_sh}^2 + V_{q\_sh}^2} \dots\dots\dots (2.37)$$

$$\alpha_{sh} = \tan^{-1} \frac{V_{q\_sh}}{V_{d\_sh}} \dots\dots\dots (2.38)$$

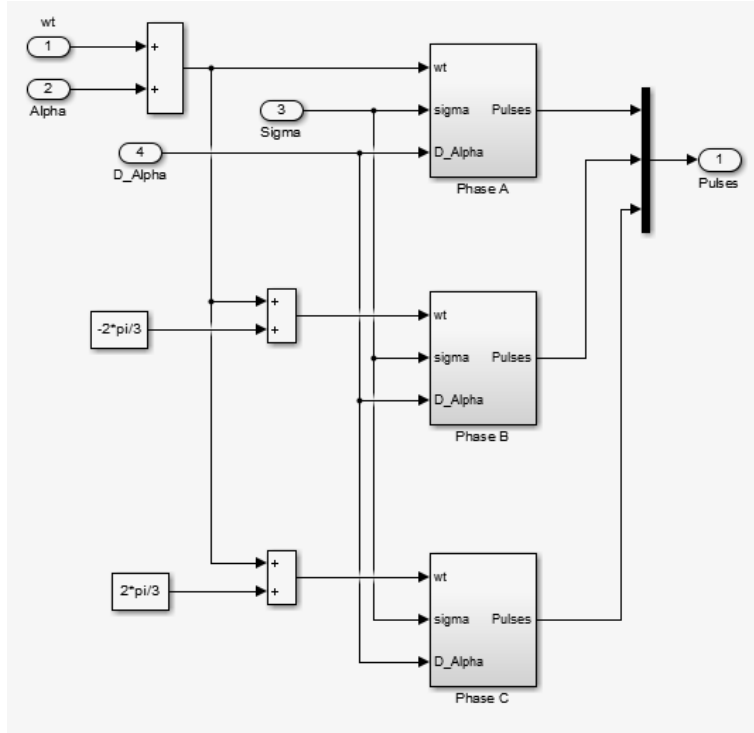


Figure 2.20: Sinusoidal pulse width modulation for shunt converter

### 2.3.3 Series controller of a UPFC base on FLC

for the series controller, its working principle is similar to shunt controller, the only difference is that the series controller is controlling the active and reactive power flow through distribution feeder, as it shown in Fig. 2.21. As the line current has magnitude and the angle which are controllable. The actual values of the active and reactive power through the transmission line  $P_{act}$  and  $Q_{act}$  is measurement and then subtraction of these values from their reference  $P_{ref}$  and  $Q_{ref}$  values is done to get the error values  $P_{error}$  and  $Q_{error}$ . Then, the error rate for the obtained error signals  $P_{error\_rate}$  and  $Q_{error\_rate}$  are calculated and then these values are set as inputs to the two FLC [52]. Using equation (2.39) and (2.40) to compute  $q$  and  $d$  components for the injected voltage.

$$V_{mag\_se} = \sqrt{V_{d\_se}^2 + V_{q\_se}^2} \dots\dots\dots (2.39)$$

$$\alpha_{se} = \tan^{-1} \frac{V_{q_{se}}}{V_{d_{se}}} \dots\dots\dots (2.40)$$

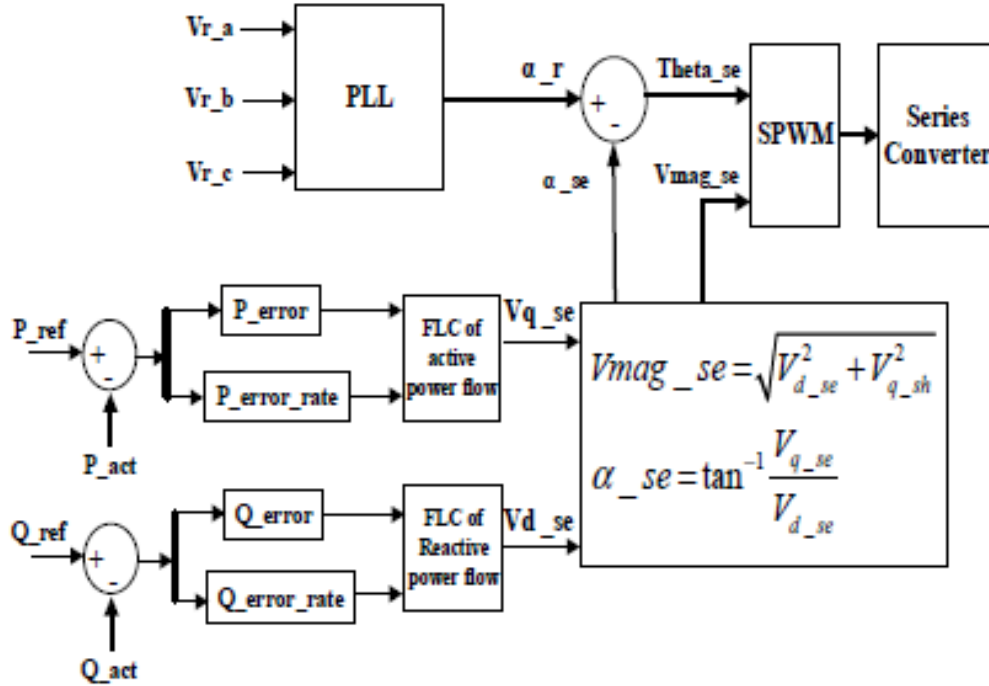


Figure 2.21: Series controller of sending-end voltage and DC link voltage to generate  $(V_{mag-se})$  and  $(\alpha_{se})$  [51]

## 2.4 Prevention of voltage instability

Some of the causes for occurrence of voltage instability includes:

- Different in Transmission of Reactive Power Under Heavy Loads.
- High Reactive Power Consumption at Heavy Loads.
- Occurrence of Contingencies.
- Voltage sources are too far from load centers.
- Due to unsuitable locations of FACTS controllers.
- Poor coordination between multiple FACTS controllers.
- Presence of Constant Power Loads.
- Reverse Operation of ON Load Tap-Changer (OLTC).

Some of the prevention of voltage instability problem by following:

- Placement of Series and Shunt Capacitors.
- Installation of Synchronous Condensers.
- Placement of FACTS Controllers.
- Coordination of Multiple FACTS Controllers.
- Under-Voltage Load Shedding.
- Blocking of Tap-Changer Under Reverse Operation.
- Generation Rescheduling.

## **2.5 Reason for choosing UPFC**

Among all different types of FACTS, UPFC has the capability to monitor all parameters influencing the transmission line's power flow including: Voltage magnitude, impedance of the line and bus angle. The composite characteristics are normally such that a load bus absorbs reactive power. Both active and reactive powers of the composite loads vary due to voltage magnitude [53] Overhead lines and underground cables are able to supply or absorb reactive power depending on the load current whereby below surge impedance load, they supply and above surge impedance load, they absorb reactive power [54] Irrespective of the loading of the transformer, the Transformers always absorb reactive power; when the transformer is operating at no load, the shunt magnetizing reactance effects dominate and if its operating at full load, the series leakage inductance effects dominate therefore the UPFC is responsible in supplying the reactive power thus boosting local voltages. The principal advantages of the UPFC are their low cost and flexibility of installation and operation. The main disadvantage of UPFC is that their reactive power output is proportional to the inverse of the square of the voltage. In [55] a synchronous condenser is a synchronous motor running without a prime mover or a mechanical load which by controlling the field excitation can be made to either generate or absorb reactive power. For proper voltage control, the synchronous motor is used hand in hand with a voltage regulator. The condenser is flexible to operate for all load conditions and its reactive power output is not a function of system voltage. However, synchronous condensers are expensive to install and it is difficult to increase their capacity. As it known

that in UPFC there is a SSSC, static series capacitors are connected in series with line conductors to reduce the inductive reactance between supply and load for improved power transfer capability. The drawbacks of series capacitors are ferro resonance switching in of unloaded transformer at the end of a series compensated line and locking of induction motors [56]. It is investigated that the UPFC is the effective FACTS device for stability enhancement at a shortest minimum of time see table 2.3 below.

*Table 2.3: Comparison of FACTS devices for power system stability enhancement*

| Two-area power system with |  | Is FACTS has ability to enhance power system stability? |  | Settling time in post fault period (in seconds) |  |
|----------------------------|--|---------------------------------------------------------|--|-------------------------------------------------|--|
|                            |  |                                                         |  |                                                 |  |
| STATCOM                    |  | Yes                                                     |  | 0,4                                             |  |
| SVC                        |  | Yes                                                     |  | 0,7                                             |  |
| TCSC                       |  | Yes                                                     |  | 0,5                                             |  |
| UPFC                       |  | Yes                                                     |  | 0,3                                             |  |

## 2.6 Load flow solution

### 2.6.1 Introduction

Load flow studies and analysis in power system are most important aspects especially for power system planning, and reconfigurations. Its contribution is to produce the sinusoidal steady state of the complete system network such as: load flow-voltage magnitude (express in per-unit), load flow angle on each bus, reactive and active power, power generated, power consumed by the end users, and power losses along the way. The steady state real and reactive powers supplied by a bus in a power network are expressed in terms of nonlinear algebraic equations. *MATLAB* uses iterative methods for solving the following equations on (2.6.2).



### 2.6.2 Load flow formulation

In a three-phase balanced system, the system can be represented as single line equivalent diagram, see Fig.2.22 below. The nodal analysis is used to derive two load equations namely:

- Gauss-Siedel [G-S] method
- Newton-Raphson [N-R] method

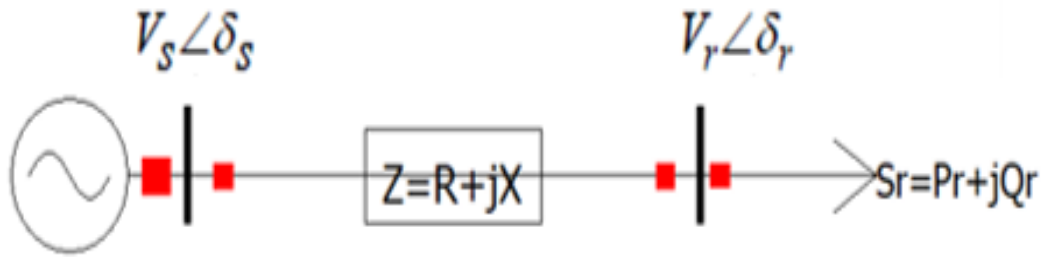


Figure 2.22: Single line diagram of distribution network

In transmission line, the relationship between voltage (V) and current (I) in any bus is determined by:

$$I = Y.V \dots\dots\dots(2.41)$$

Y is the admittance from bus to bus given as:  $Y_{i,j}$ , therefore equation (2.41) can be expanded in that form:

$$I = \sum_{i=1}^n Y_{i,j}.V_i \dots\dots\dots(2.42)$$

As complex power  $S = V.I^*$ , equation (2.42) can be developed in terms of power.

$$I = \frac{S^*}{V^*} \dots\dots\dots(2.43)$$

And

$$S_{ij} = P_i - Q_j \dots\dots\dots(2.44)$$

Therefore, Gauss-Siedel equation is obtained by substitute equation (2.42), (2.43), (2.44) and make Voltage as subject of the formula.

$$V_i = \frac{1}{y_{i,i}} \left[ \frac{P_i - jQ_i}{V_i^*} - \sum_{j=1, j \neq i}^n y_{i,j} V_j \right] \dots\dots\dots(2.45)$$

Then, by splitting equation (2.42) in to two equations as follows, Newton-Raphson is obtained.

$$P_i = \sum_{j=1}^n |V_i| |y_{i,j}| |V_j| \cos(\theta_{i,j} + \delta_i - \delta_j) \dots\dots\dots(2.46)$$

$$Q_i = -\sum_{j=1}^n |V_i| |y_{i,j}| |V_j| \sin(\theta_{i,j} + \delta_i - \delta_j) \dots\dots\dots(2.47)$$

Equations (2.46) and (2.47) represent Newton-Raphson method of analysing load flow. In this study, this method is used as it produces accurate solutions in terms of converging iterations and its very faster than the Gauss-Siedal method.

### 2.6.3 Steps to solve the Newton Raphson (N-R) algorithm

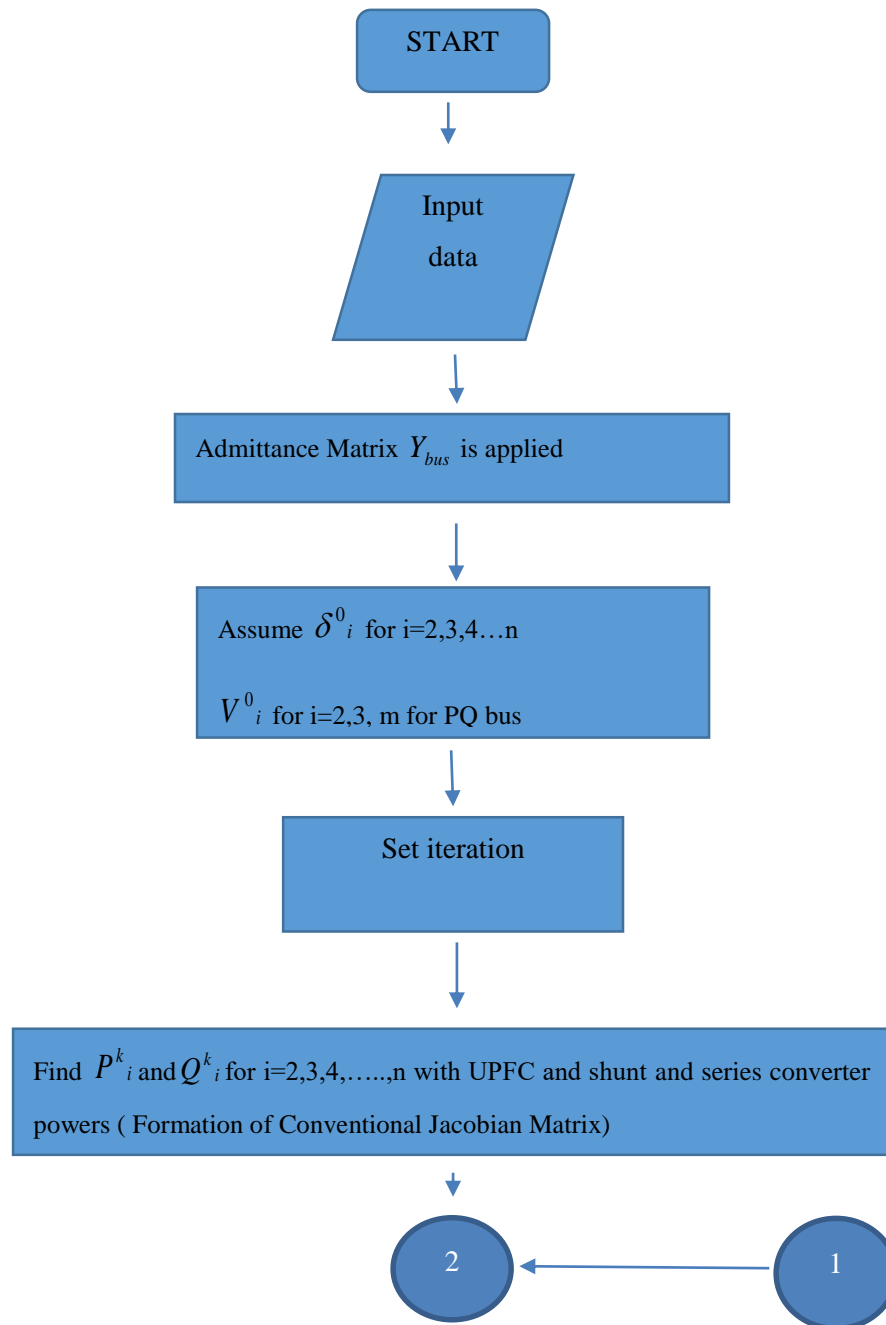


Figure 2.23: Flow Chart for load flow by Newton Raphson with UPFC (cont...)

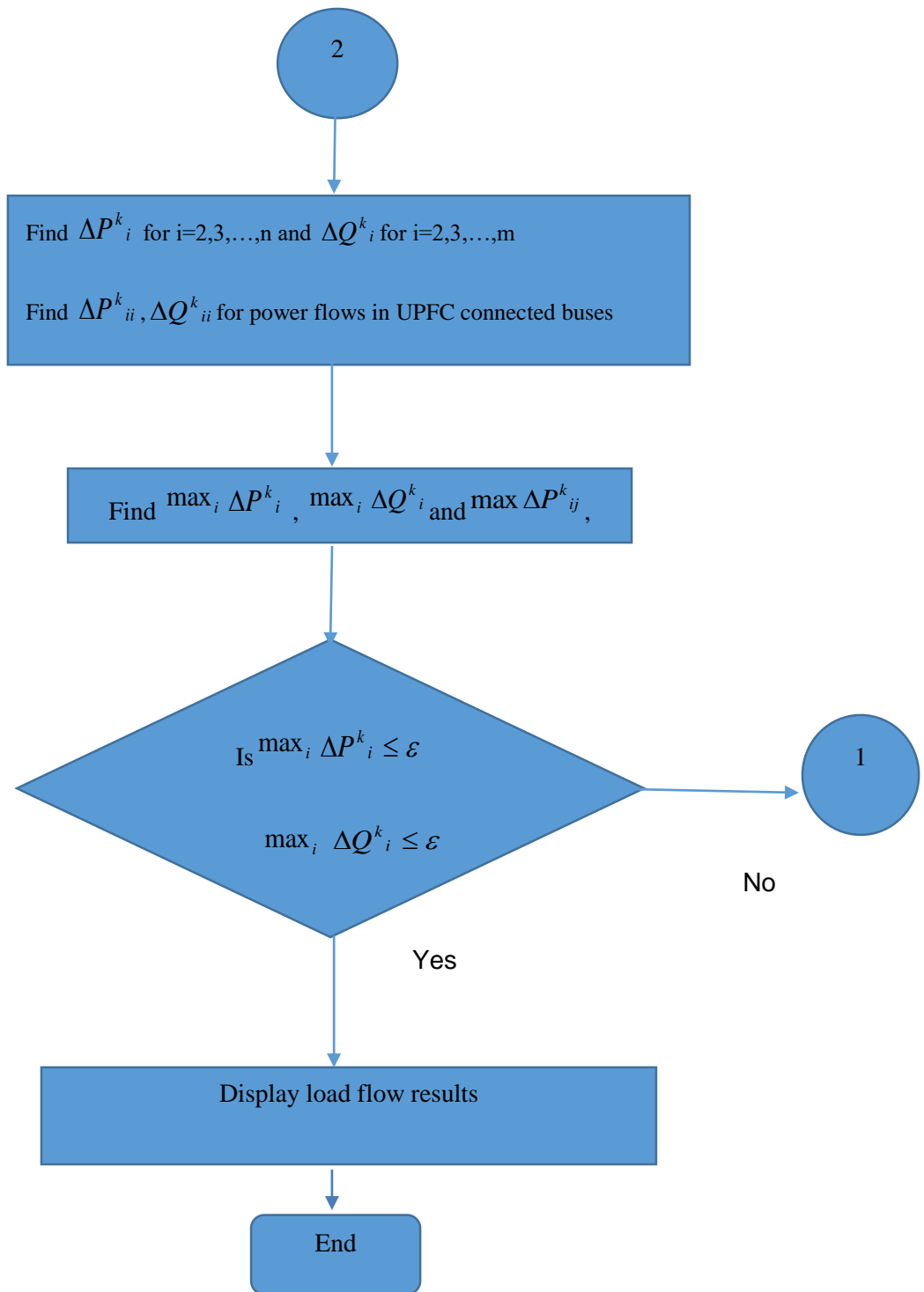


Figure 2.23: Flow Chart for load flow by Newton Raphson with UPFC

# CHAPTER THREE

## RESEARCH METHODOLOGY

### 3.1 Introduction

Voltage collapse has been documented as a serious threat to the power system stability and for its operation. Due to unexpected load increases or insufficient reactive power supply, voltage violations and undesirable line outages might be unavoidable when power systems operated close to its transmission capacity limits. The ability to draw a clear and complete picture of system voltage stability with accurate indications and precise voltage collapse allocations allow operators to take the necessary action to prevent such incidents. A successful avoidance of such system collapse is based on method's accuracy, speed of indication, and very low computation time [57]. This chapter is focusing mainly on the efficient method for conducting line voltage stability analysis in power systems which is a Voltage Stability Index (VSI). The beauty of this developed method is: accurate, fast, simple, and theoretically proven for determining the exact voltage collapse points and also for determining the line that is highly stressed. Parenthetically, there are various types of indices of which will be discuss in detailed shortly such as: Line Stability Factor (LQP), Voltage Collapse Point Indicator (VCPI), Line Stability Index (Lmm), Performance Voltage Stability Index (PVSI) and Fast Voltage Stability Index (FVSI).

### 3.2 Line stability indices

The above mentioned Line stability indices are expressed in a single line diagram, based on the concept of power transmission. In Fig.3.1, a single line diagram is shown in an interconnected network.

Where,

$V_s$  and  $V_r$  are the sending end and receiving end voltages

$\delta_s$  and  $\delta_r$  are the phase angle at the sending and receiving buses

$Z$  : is the impedance of the line

$R$  : is the resistance of a conductor material

$\theta$  : is the line impedance angle

$X$  : is the line reactance

$Q_r$  : is the reactive power at the receiving end

$P_r$  : is the active power at the receiving end.

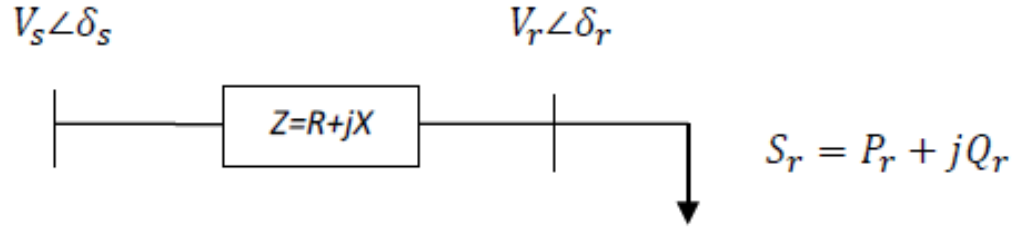


Figure 3.1: Two bus system

### 3.2.1 VCPI index

The Voltage Collapse Point Indicators (VCPI) is proposed in [58] are based on the concept of maximum power transferred through a line. VCPI development in *MATLAB* software is shown in Fig. 3.2 below.

$$VCPI_{(P)} = \frac{P_r}{P_{r(\max)}} \dots\dots\dots(3.1)$$

$$VCPI_{(Q)} = \frac{Q_r}{Q_{r(\max)}} \dots\dots\dots(3.2)$$

From the equations above, the numerator is the active or reactive power transferred to the receiving end of the line and it depends on system parameters, network topology, interconnections and load demand of the system.

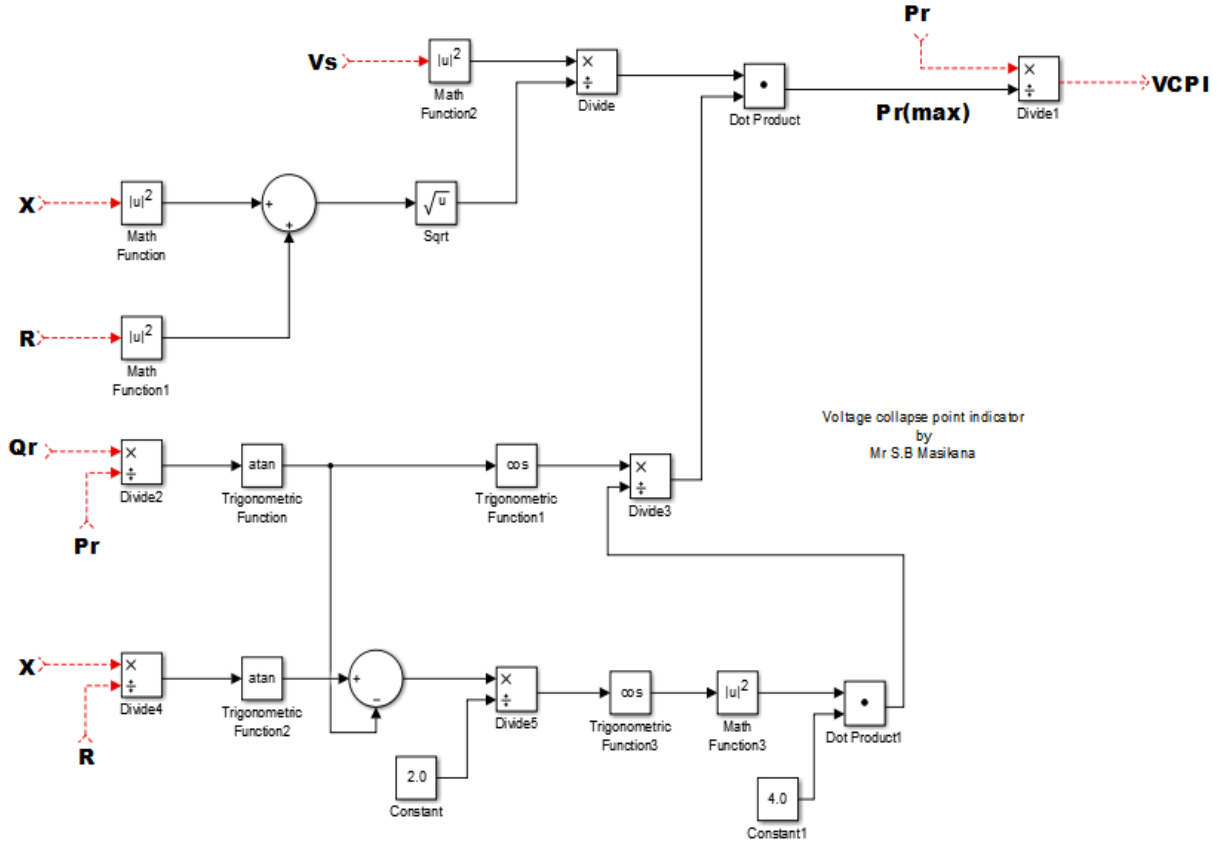


Figure 3.2: VCPI development

The denominator is the maximum power that can be transferred to the receiving end at a particular instant. It can be expressed as:

$$P_{r(\max)} = \frac{V_s^2}{Z} \cdot \frac{\cos \phi}{4 \cos^2 \left( \frac{\theta - \phi}{2} \right)} \dots \dots \dots (3.3)$$

$$Q_{r(\max)} = \frac{V_s^2}{Z} \cdot \frac{\sin \phi}{4 \cos^2 \left( \frac{\theta - \phi}{2} \right)} \dots \dots \dots (3.4)$$

Where  $\phi = \tan^{-1} \left( \frac{Q_r}{P_r} \right)$

### 3.2.2 Lmn index

The Line Stability Index is proposed in [59] is based more on the concept of power flow through a single line network and adopting the technique of analysing a power system as a single line network. As it observed in Fig.3.1 that this VSI is used to find the stability index for each line connection between two bus bars in an interconnected network.

From power flow equations, apparent power is given as:

$$S_r = \frac{|V_s||V_r|}{Z} \angle(\theta - \delta_s + \delta_r) - \frac{|V_r|^2}{Z} \angle \theta \dots\dots\dots(3.5)$$

As it known that in the apparent power there is active and reactive power, then the equation (3.5) can be separated as:

$$P_r = \frac{V_s \cdot V_r}{Z} \cos(\theta - \delta_s + \delta_r) - \frac{V_r^2}{Z} \cos \theta \dots\dots\dots(3.6)$$

$$Q_r = \frac{V_s \cdot V_r}{Z} \sin(\theta - \delta_s + \delta_r) - \frac{V_r^2}{Z} \sin \theta \dots\dots\dots(3.7)$$

Where  $\delta = \delta_s - \delta_r$

$$\text{Then } V_r = \frac{V_s \sin(\theta - \delta) \pm \{[V_s \sin(\theta - \delta)]^2 - 4ZQ_s \sin \theta\}^{0.5}}{2 \sin \theta} \dots\dots\dots(3.8)$$

By substituting  $Z \sin \theta = X$

Therefore

$$L_{mn} = \frac{4XQ_r}{[V_s \sin(\theta - \delta)]^2} \leq 1 \dots\dots\dots(3.9)$$

This VSI should not exceed 1, if  $L_{mn}$  is more than 1 that means the system is unstable.

The Fig. 3.3 below showing the  $L_{mn}$  development.



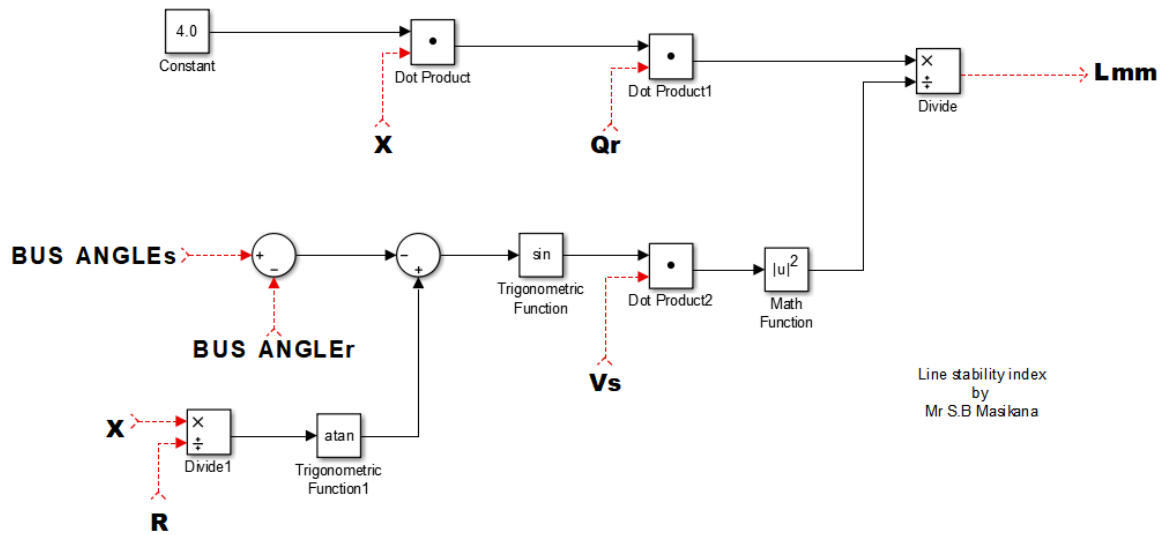


Figure 3.3: Lmn development

### 3.2.3 LQP index

The line stability Factor (LQP) is described in [60], it is similar to the previous index Lmn and is calculated as given in Fig. 3.4 follows:

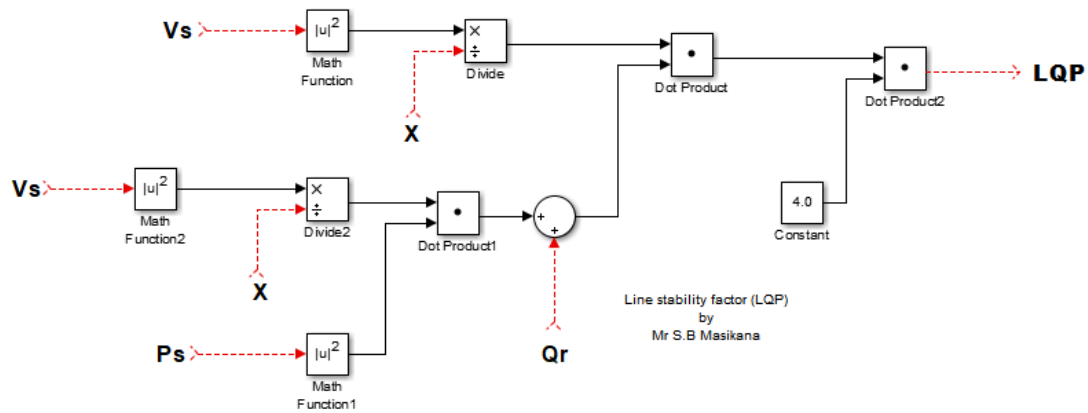


Figure 3.4: LQP development

$$LQP = 4 \left( \frac{X}{V_i^2} \right) \left( \frac{X}{V_i^2} P_i^2 + Q_j \right) \leq 1 \dots\dots\dots (3.10)$$

### 3.2.4 FVSI index

This index FVSI is also based on the concept of power flow through a single line network. It is developed starting by considering the sending end bus as the reference and using the standard current equation:

$$I = \frac{V_s \angle 0 - V_r \angle \delta}{R + jX} \dots\dots\dots(3.11)$$

And the above index is calculated as:

$$FVSI = \frac{4Z^2 \cdot Q_r}{V_s^2 \cdot X} \dots\dots\dots(3.12)$$

### 3.2.5 PVSI index

In power system, when analysing the voltage stability usually starts by running a power flow solution to compute the voltage magnitude at each node and angles.

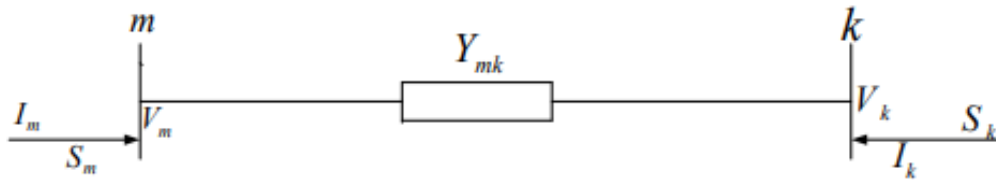


Figure 3.5: showing two currents entering the bus

In Fig. 3.5 it is observed that the current injected into a node m in terms of real and reactive power is given as:

$$I_m = \left( \frac{P_m + jQ_m}{V_m} \right) \dots\dots\dots(3.13)$$

In [61] is where the power flow equations by Newton Raphson iterative technique is depicted in detailed. In a compact form, the new voltage magnitude at a bus m can be updated as:

$$\delta_m^{(r+1)} = \delta_m^{(r)} + \Delta\delta_m^{(r)} \dots\dots\dots(3.14)$$

$$|V_m^{(r+1)}| = |V_m^{(r)}| + \Delta|V_m^{(r)}| \dots\dots\dots(3.15)$$

Where  $r$  is the number of iteration

By considering the bus voltage magnitudes obtained from (3.15), the absolute values are taken and changed into per-unit. Consequently, the performance voltage stability index (PVSI) with respect to reactive power load variations at each load node is given as:

$$(PVSI_v) = \sum_{m=1}^n \left( \frac{V_{nom} - V_m}{V_{nom}^{lim}} \right)^2 \dots\dots\dots(3.16)$$

Where  $n$  represent the total number of load nodes;

$V_{nom}$  is the rated or nominal voltage magnitude;

$V_m$  is the bus voltage magnitude;

$V_{nom}^{lim}$  is the voltage deviation limit which is the average of  $V_{nom}$  and  $V_m$  ;

$k$  is the reactive power loading condition.

### 3.3 Table summary

The table of summary is depicted in Table 3.1 with the aim of giving the reader a clear overview on the voltage stability indices. This table summary presents the classifications of indices, the equations to compute them and their stability conditions (stable and unstable).

Table 3.1: Table summary

|                                  | Name | Index Calculation                                                                   | Unstable condition | Stable condition |
|----------------------------------|------|-------------------------------------------------------------------------------------|--------------------|------------------|
| <b>System Variable-based VSI</b> | VCPI | $VCPI_{(P)} = \frac{P_r}{P_{r(max)}}$                                               | $VCPI > 1$         | $VCPI \leq 1$    |
|                                  | Lmn  | $L_{mn} = \frac{4XQ_r}{[V_s \sin(\theta - \delta)]^2}$                              | $Lmn > 1$          | $Lmn \leq 1$     |
|                                  | LQP  | $LQP = 4 \left( \frac{X}{V_i^2} \right) \left( \frac{X}{V_i^2} P_i^2 + Q_j \right)$ | $LQP > 1$          | $LQP \leq 1$     |
|                                  | FVSI | $FVSI = \frac{4Z^2 \cdot Q_r}{V_s^2 \cdot X}$                                       | $FVSI > 1$         | $FVSI \leq 1$    |
|                                  | PVSI | $(PVSI_v) = \sum_{m=1}^n \left( \frac{V_{nom} - V_m}{V_{lim}} \right)^2$            | $PVSI > 1$         | $PSVI \leq 1$    |
|                                  |      |                                                                                     |                    |                  |
|                                  |      |                                                                                     |                    |                  |

### 3.4 Conclusion

In this section, a method of analysing a voltage stability is presented which compute the voltage analysis precisely at each distribution feeder to determine the collapse point on the distribution system. This proposed method indicates how far the distribution feeder is from a severe load condition or collapse point, permitting separate analysis if one feeder is highly stressed. This method crafted in order to relate sending end voltage and the receiving end voltage, permitting more effective stability analysis, particularly when the power system is subjected to a sudden increase in load power demands. This proposed method is accuracy in conducting line voltage stability analysis and its predictions of voltage collapse were tested.

## CHAPTER FOUR

### SIMULATION AND ANALYSIS

#### 4.1 Test system description

This section is focussing more on the modelling, simulation and analysis of an IEEE-15 bus test system which is use for the present study. The IEEE-15 bus distribution feeder model represented in the form of a single line diagram and shown in Fig. 4.1 and it is simulated using standard *MATLAB* software. The system is consisting of 15-buses, 13-loads connected, and 14-lines. The IEEE-15 bus distribution feeder is consisting of the following data:

- Number of buses=15
- Slack bus=01
- Number of lines=14
- Base voltage=11KV
- Base power=100KVA
- Tolerance limit=0.001

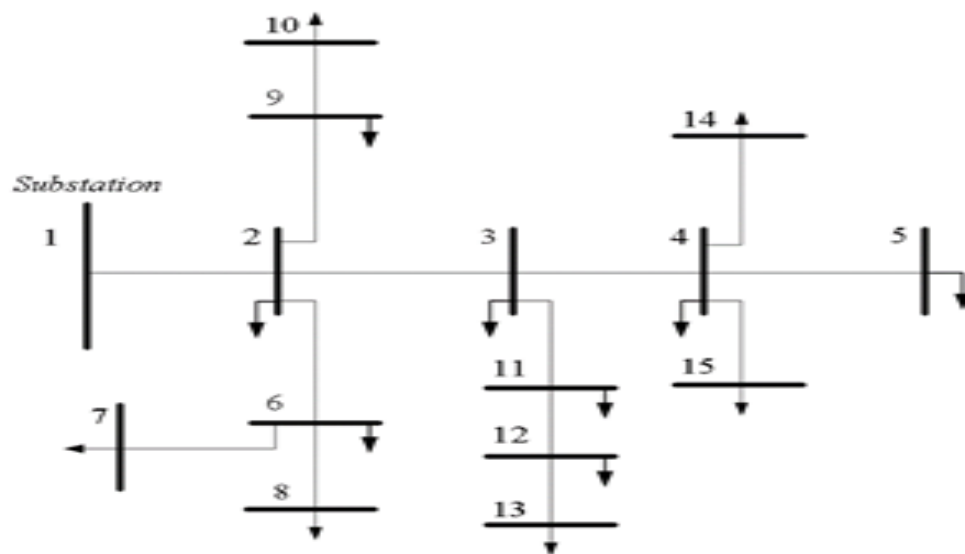


Figure 4.1: IEEE-15 bus distribution feeder [62]

## 4.2 Distribution feeder (Line)

In power system, at the secondary side of the transmission line is a distribution feeder which is employed to convey electric power from transmission line to service mains of the consumers. The distribution feeder is made up of conductors, as conductor has a resistivity ( $\rho$ ), at a certain length ( $l$ ), and the cross-sectional area ( $A$ ) these parameters produces the resistance of the conductor material which is not physical as expressed:

$$R = \frac{\rho l}{A} [\Omega] \dots\dots\dots(4.1)$$

When the conductor is carrying a current the magnetic field builds-up that gives the effect of an inductive reactance  $X$ , which is given as:

$$X = 2\pi \cdot f \cdot l [\Omega] \dots\dots\dots(4.2)$$

Because resistance and reactance are in series in a line as it shown in Fig.4.2, they sum each other to give impedance, hence the distribution feeder is always represented as  $Z$ .

$$Z = R + jX_L [\Omega] \dots\dots\dots(4.3)$$

The inductance of the line is measured by the induced electrical voltage compared to the rate of electric current change [63]. It is an electrical property which represents the flux linkage in conductors.

$$L = \frac{\lambda}{I} [H] \dots\dots\dots(4.4)$$

Where:

$L$  : Inductance [H]

$\lambda$  : Instantaneous flux linkage [Wb]

$I$  : Current [A]

The line capacitance is characterized as the charge on the conductors which is the result of the voltage difference between the conductors of the line feeder and to ground [63] expressed as:

$$C = \frac{q}{v} [F] \dots\dots\dots(4.5)$$

Where:

$C$  : Capacitance of the line [F]

$v$  : Potential difference between two conductors [V]

$q$  : Charge on the conductor [C]

To set up the distribution feeder lines for load flow investigation purposes, four parameters are considered such as; resistance, inductance, capacitance, and conductance, these are the parameters which influence the line capacity as a part of the power system. Resistance, inductance, and capacitance are only considered in this section while the conductance is dismissed on the grounds that its contribution to shunt admittance is negligible [64,65]. Resistance or effective resistance represents the power losses in a conductor. The effective resistance of a conductor is the result of power losses (W) in the conductor divided by the current (A) square [63].

$$W = I^2 R [W] \dots\dots\dots(4.6)$$

Make resistance as a subject of the formula and combine with (4.1)

$$R = \frac{P_{Losses}}{I^2} = \frac{pl}{A} \dots\dots\dots(4.7)$$

In Fig. 4. 2, the main parameters (R, L, and C) which are measured based on unit length,  $\Omega/\text{km}$  for resistance,  $\text{mH}/\text{km}$  for inductance and  $\mu\text{F}/\text{km}$  for capacitance are implemented within the *MATLAB* software tool. The capacitance of the line is divided into two halves per kilometre; one half being lumped at the receiving end and other is lumped at the sending end of the line. It is obvious that capacitance at the sending end has no effect

on the line drop. However, its charging current must be added to line current in order to obtain the total sending end current [66].

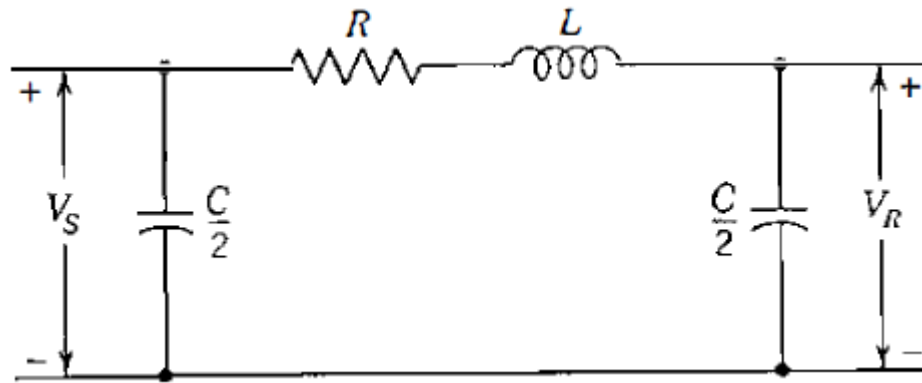


Figure 4.2: Single-phase equivalent circuit of a medium length line [67]

In any four terminal electrical network, the input voltage and current can be expressed in terms of output voltage and current. Similarly, the above network is a four terminal network with constants (ABCD); two input entering the network and other two are leaving the network. *MATLAB* software derive expression from matrix;

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_R \\ I_R \end{bmatrix} \dots\dots\dots (4.8)$$

Therefore,  $V_s$  and  $I_R$  inputs can be expressed as:

$$V_s = AV_R + BI_R \dots\dots\dots (4.9)$$

$$I_s = CV_R + DI_R \dots\dots\dots (4.10)$$

Where:

$V_s$  : Sending end voltage

$I_s$  : Sending end current

$V_R$  : Receiving end voltage

$I_R$  : Receiving end current

For constants ABCD, it is derived that;



$$A = D = \left[ 1 + \frac{Y.Z}{2} \right] \dots\dots\dots(4.11)$$

Where:

$Y$  : is the admittance of the line [U]

$Z$  : is the impedance of the line [ $\Omega$ ]

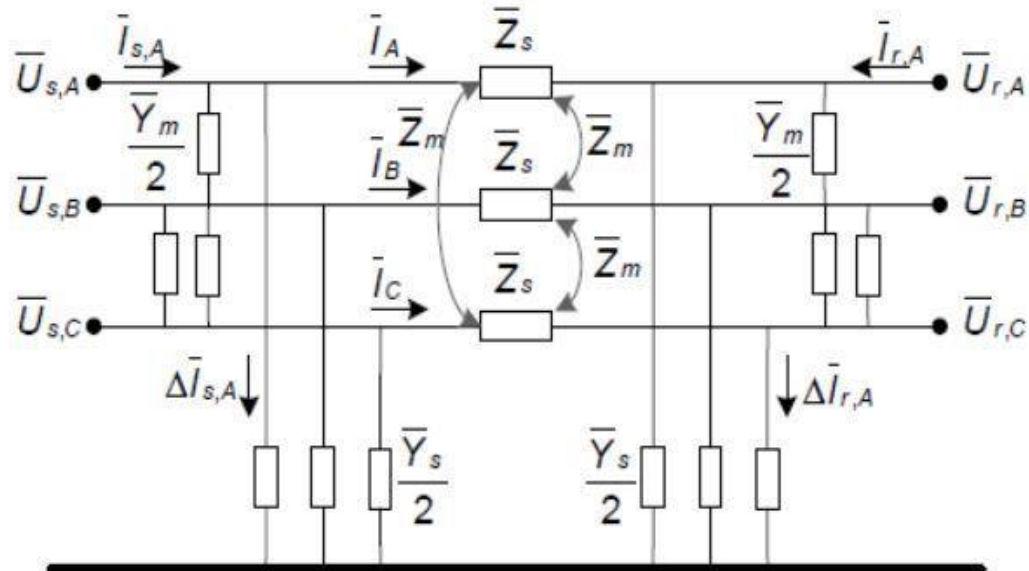


Figure 4.3: Network of a lumped parameter model of a balanced three-phase lines

$$B = Z[\Omega] \dots\dots\dots(4.12)$$

$$C = Y \left[ 1 + \frac{Y.Z}{4} \right] [\Omega] \dots\dots\dots(4.13)$$

#### 4.2.1 Case study of an IEEE-15 bus system

Further, Appendix A1 and A2 shows the line data table as well as load data table for simulated IEEE 15 bus system.

### 4.3 Modelling and simulation of an IEEE-15 bus system under study

The load data will exponentially increase in stairs steps of 10% up to 40% without UPFC placement to identify the weakest bus or the bus that is highly stressed, then UPFC should be placed at that bus in order to improve the voltage profile and the quality of the entire network. Simulation studies will be done for different scenarios in IEEE-15 bus distribution feeder network. Five different scenarios are considered for the present study which are as follows:

- Scenario 1: The network is running on a normal load condition (base case).
- Scenario 2: 10% load increase without UPFC.
- Scenario 3: 20% load increase without UPFC.
- Scenario 4: 30% load increase without UPFC.
- Scenario 5: 40% load increase without UPFC.

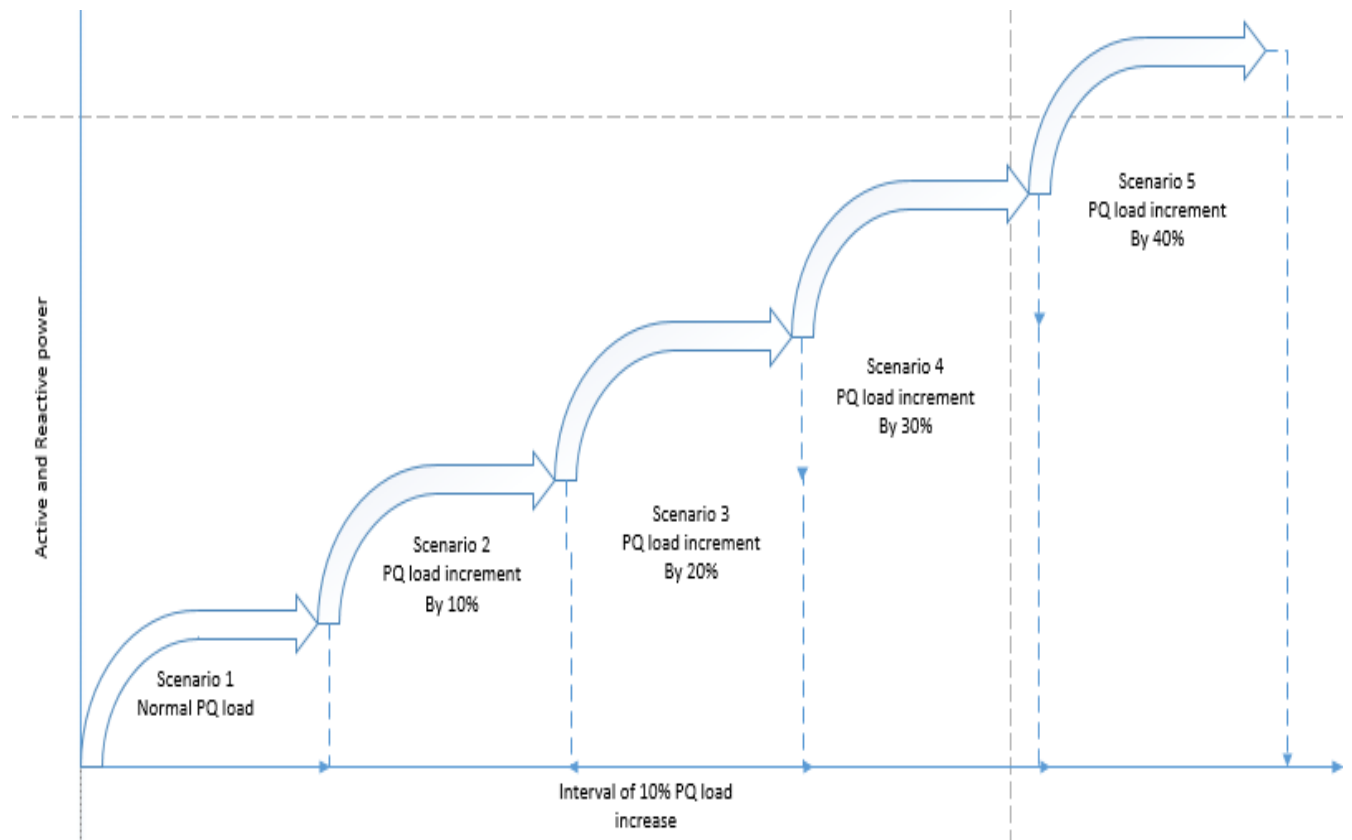


Figure 4.4: Showing the PQ load increase up to 40% without UPFC placement

#### 4.3.1 Load flow study without UPFC placement

*MATLAB* with the load flow tool will conduct the investigation by computing and converge the system without mismatch in the iterations. *MATLAB* software is operating using Newton-Raphson method which is fastest method. For the normal load to 30% load increase, the load flow converged in 4 iterations without a mismatch in the iterative procedure. And at 40% load increase, the load flow converged in 5 iterations. For the load flow computation, the simulation shows what is being generated, load consumed, and the grid losses in terms of active and reactive power. The following tables from 4.1 to 4.5 shows the summary for all scenarios.

*Table 4.1: Load flow summary for scenario 1*

| <b>Normal load</b> |                          |                              |
|--------------------|--------------------------|------------------------------|
| <b>System</b>      | <b>Active power (MW)</b> | <b>Reactive power (MVar)</b> |
| Total generation   | 0.43                     | 0.25                         |
| Total PQ load      | 0.43                     | 0.23                         |
| Total grid losses  | 0.00                     | 0.02                         |

*Table 4.2: Load flow summary for scenario 2*

| <b>10% load increase</b> |                          |                              |
|--------------------------|--------------------------|------------------------------|
| <b>System</b>            | <b>Active power (MW)</b> | <b>Reactive power (MVar)</b> |
| Total generation         | 0.47                     | 0.26                         |
| Total PQ load            | 0.46                     | 0.25                         |
| Total grid losses        | 0.01                     | 0.01                         |

*Table 4.3: Load flow summary for scenario 3*

| <b>20% load increase</b> |                          |                              |
|--------------------------|--------------------------|------------------------------|
| <b>System</b>            | <b>Active power (MW)</b> | <b>Reactive power (MVar)</b> |
| Total generation         | 0.52                     | 0.23                         |
| Total PQ load            | 0.51                     | 0.28                         |
| Total grid losses        | 0.01                     | -0.04                        |

Table 4.4: Load flow summary for scenario 4

| 30% load increase |                   |                       |
|-------------------|-------------------|-----------------------|
| System            | Active power (MW) | Reactive power (MVar) |
| Total generation  | 0.56              | 0.22                  |
| Total PQ load     | 0.55              | 0.22                  |
| Total grid losses | 0.01              | 0.00                  |

Table 4.5: Load flow summary for scenario 5

| 40% load increase |                   |                       |
|-------------------|-------------------|-----------------------|
| System            | Active power (MW) | Reactive power (MVar) |
| Total generation  | 0.62              | 0.09                  |
| Total PQ load     | 0.61              | 0.33                  |
| Total grid losses | 0.01              | -0.25                 |

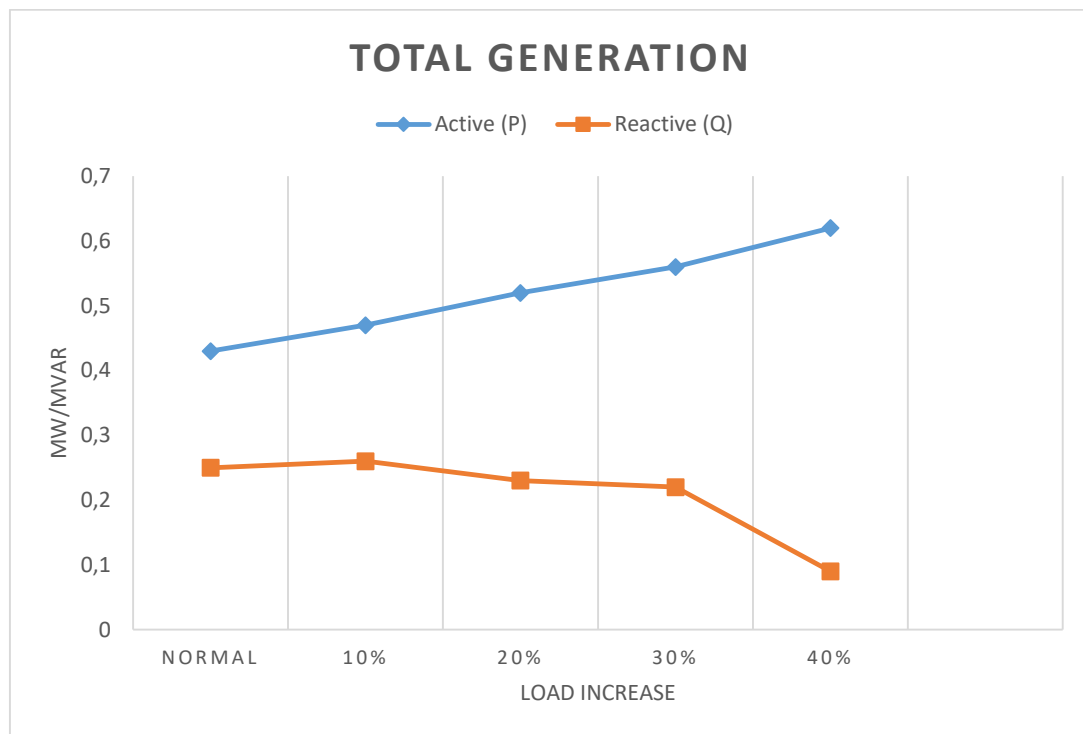


Figure 4.5: Total PQ generated before UPFC placement

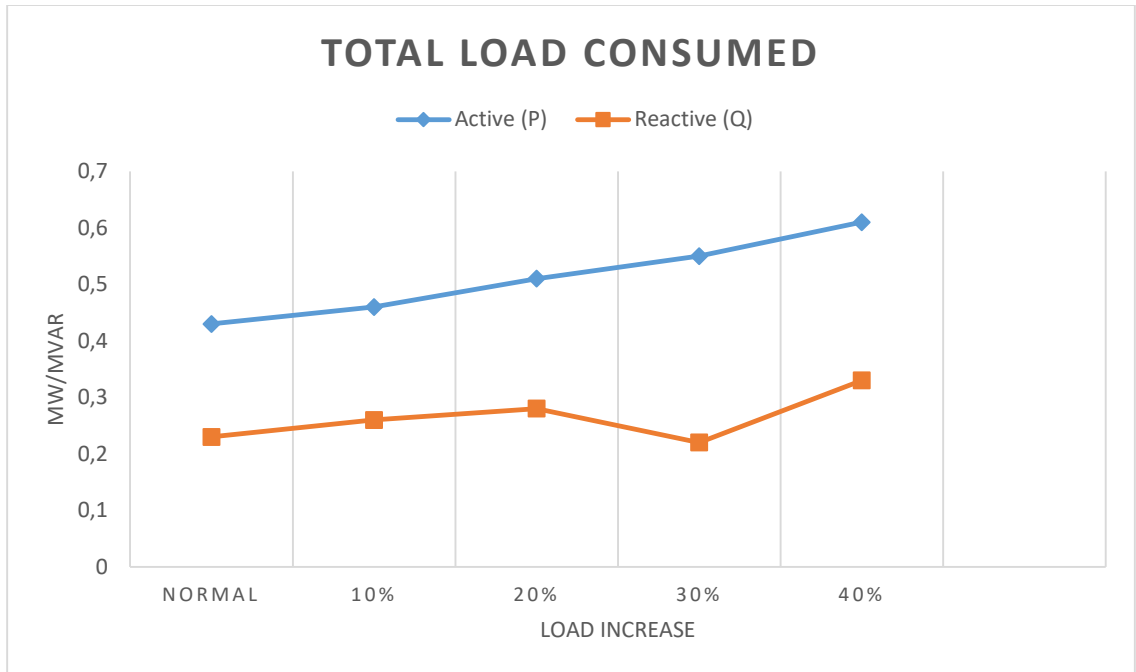


Figure 4.6: Total PQ load consumed before UPFC placement

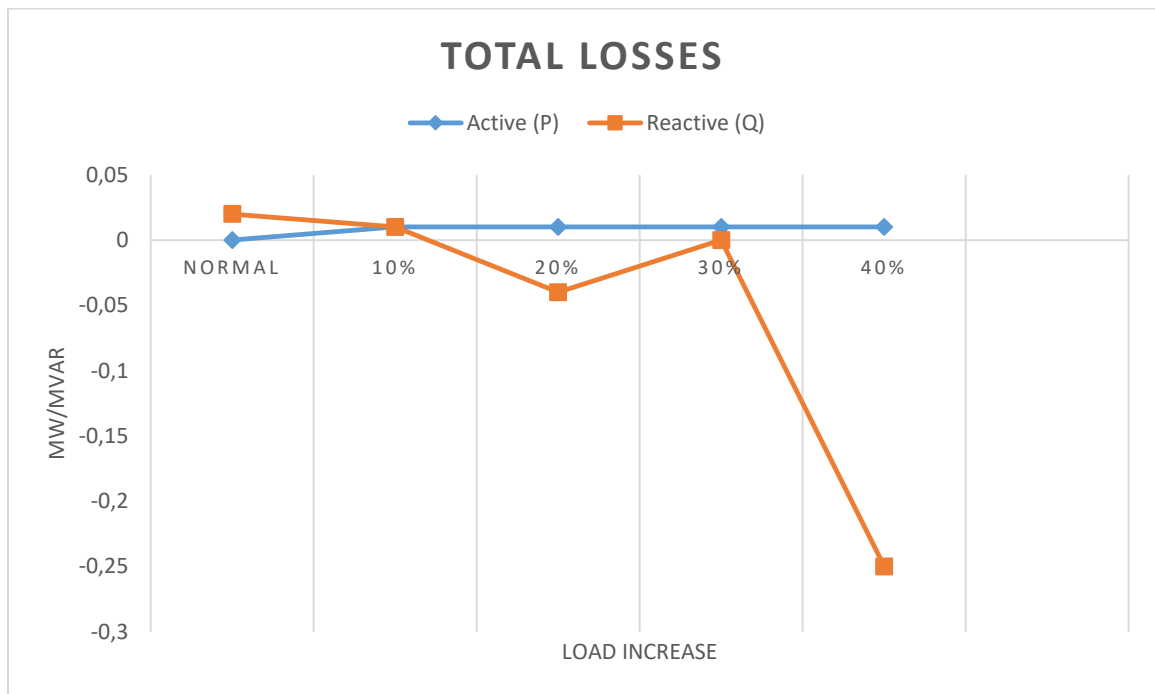


Figure 4.7: Total losses before UPFC placement

#### 4.3.2 PQ load at 10% load increase without UPFC placement

Table 4.6: Data for 10% load increase without UPFC

| At 10% load increase |                   |                       |
|----------------------|-------------------|-----------------------|
| Bus No               | Active power (kW) | Reactive power (kVAr) |
|                      |                   |                       |
| Bus 3                | 40,956            | 23,1                  |
| Bus 4                | 4,474             | 1,694                 |
| Bus 5                | 76,23             | 41,38                 |
| Bus 6                | 30,492            | 16,94                 |
| Bus 7                | 8,131             | 3,85                  |
| Bus 8                | 144,144           | 80                    |
| Bus 9                | 42,042            | 23,1                  |
| Bus 10               | 60,984            | 26,95                 |
| Bus 11               | 5,082             | 2,695                 |
| Bus 12               | 26,426            | 14,284                |
| Bus 13               | 14,23             | 7,7                   |
| Bus 14               | 9,656             | 10,78                 |
| Bus 15               | 6,098             | 3,08                  |

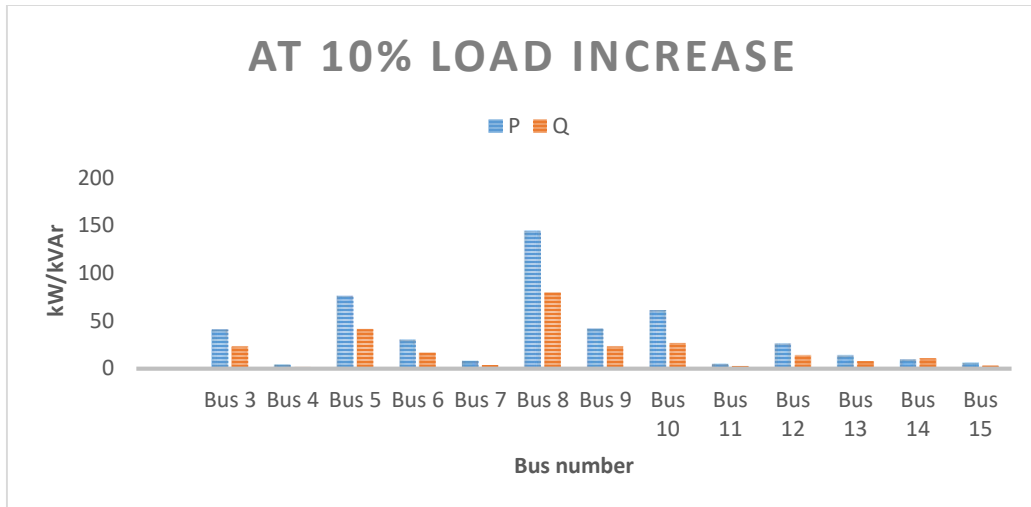


Figure 4.8: PQ load at 10% load increase without UPFC

#### 4.3.3 PQ load at 20% load increase without UPFC placement

Table 4.7: Data for 20% load increase without UPFC

| At 20% load increase |                   |                       |
|----------------------|-------------------|-----------------------|
| Bus No               | Active power (kW) | Reactive Power (kVar) |
| Bus 3                | 44,68             | 25,2                  |
| Bus 4                | 4,88              | 1,848                 |
| Bus 5                | 83,16             | 45,36                 |
| Bus 6                | 33,264            | 18,48                 |
| Bus 7                | 8,87              | 4,2                   |
| Bus 8                | 157,248           | 87,36                 |
| Bus 9                | 45,864            | 25,2                  |
| Bus 10               | 66,528            | 29,4                  |
| Bus 11               | 5,544             | 2,94                  |
| Bus 12               | 28,829            | 15,582                |
| Bus 13               | 15,523            | 8,4                   |
| Bus 14               | 10,534            | 11,76                 |
| Bus 15               | 6,653             | 3,36                  |

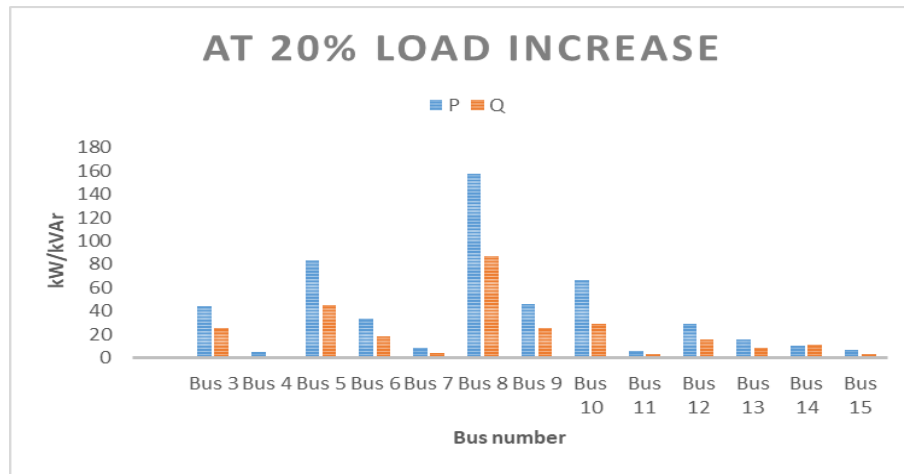


Figure 4.9: PQ load at 20% load increase without UPFC

#### 4.3.4 PQ load at 30% load increase without UPFC placement

Table 4.8: Data for 30% load increase without UPFC

| At 30% load increase |                 |                       |
|----------------------|-----------------|-----------------------|
| Bus No               | True power (kW) | Reactive power (kVAr) |
| Bus 3                | 48,403          | 27,3                  |
| Bus 4                | 5,287           | 2                     |
| Bus 5                | 90,09           | 49,14                 |
| Bus 6                | 36,036          | 20,02                 |
| Bus 7                | 9,61            | 4,55                  |
| Bus 8                | 170,352         | 94,64                 |
| Bus 9                | 49,686          | 27,3                  |
| Bus 10               | 72,072          | 31,85                 |
| Bus 11               | 6,006           | 3,185                 |
| Bus 12               | 31,231          | 16,881                |
| Bus 13               | 16,817          | 9,1                   |
| Bus 14               | 11,411          | 12,74                 |
| Bus 15               | 7,207           | 3,64                  |



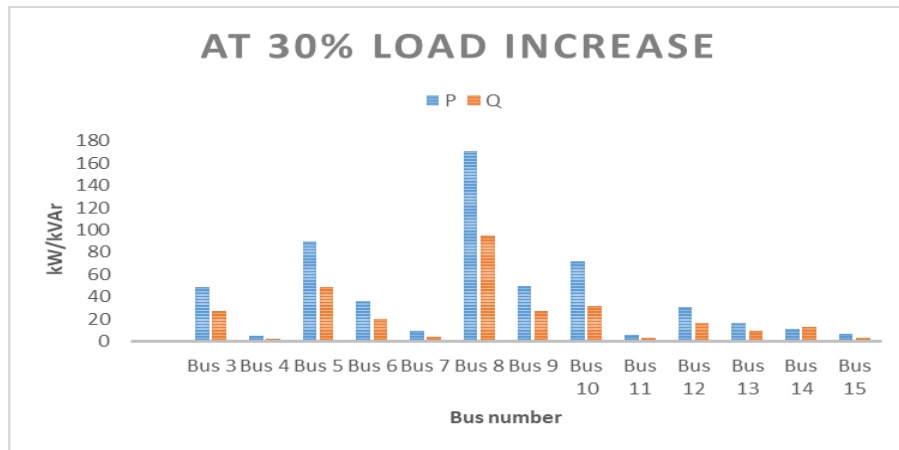


Figure 4.10: PQ load at 30% load increase without UPFC

#### 4.3.5 PQ load at 40% load increase without UPFC placement

Table 4.9: Data for 40% load increase without UPFC

| At 40% load increase |                   |                       |
|----------------------|-------------------|-----------------------|
| Bus No               | Active power (kW) | Reactive power (kVar) |
| Bus 3                | 53,19             | 30                    |
| Bus 4                | 5,8               | 2,2                   |
| Bus 5                | 99                | 54                    |
| Bus 6                | 39,6              | 22                    |
| Bus 7                | 10,56             | 5                     |
| Bus 8                | 187,2             | 104                   |
| Bus 9                | 54,6              | 30                    |
| Bus 10               | 79,2              | 35                    |
| Bus 11               | 6,6               | 3,5                   |
| Bus 12               | 34,32             | 18,55                 |
| Bus 13               | 18,48             | 10                    |
| Bus 14               | 12,54             | 14                    |
| Bus 15               | 7,92              | 4                     |

Table 4.10: Calculation and comparison of a critical bus before UPFC placement

| Bus No | Case 1   |        | Case 2   |        | Case 3   |        | Case 4   |        | Case 5   |        |
|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|--------|
|        | V_LF(Pu) | SI     | V_LF(Pu) | SI     | V_LF(Pu) | SI     | V_LF(Pu) | SI     | V_LF(Pu) | SI     |
| 1      | 1        | 0.5    | 1        | 0.5    | 1        | 0.5    | 1        | 0.5    | 1        | 0.5    |
| 2      | 0.8361   | 0.4181 | 0.8471   | 0.4236 | 0.8890   | 0.4445 | 0.9204   | 0.4602 | 1.0543   | 0.572  |
| 3      | 0.6720   | 0.336  | 0.9260   | 0.463  | 1.0907   | 0.5454 | 1.0071   | 0.5036 | 1.0486   | 0.5243 |
| 4      | 0.7820   | 0.391  | 0.7332   | 0.3666 | 0.7017   | 0.3509 | 0.7974   | 0.3987 | 0.9669   | 0.4835 |
| 5      | 0.7538   | 0.377  | 0.6934   | 0.3467 | 0.6499   | 0.3250 | 0.7539   | 0.378  | 0.5750   | 0.288  |
| 6      | 0.8307   | 0.4154 | 0.8392   | 0.4196 | 0.8812   | 0.4406 | 0.9279   | 0.464  | 1.0512   | 0.526  |
| 7      | 0.8426   | 0.4213 | 0.8510   | 0.4255 | 0.8936   | 0.4468 | 0.9411   | 0.4706 | 1.0666   | 0.533  |
| 8      | 0.7720   | 0.386  | 0.7725   | 0.3863 | 0.8123   | 0.4062 | 0.9291   | 0.4646 | 0.9895   | 0.495  |
| 9      | 0.8417   | 0.4209 | 0.8438   | 0.4219 | 0.8870   | 0.4435 | 0.9167   | 0.4584 | 1.0360   | 0.518  |
| 10     | 0.8341   | 0.4171 | 0.8328   | 0.4164 | 0.8760   | 0.4380 | 0.9047   | 0.4524 | 1.0323   | 0.5162 |
| 11     | 0.8669   | 0.4335 | 1.0669   | 0.5335 | 1.2657   | 0.6329 | 1.1603   | 0.5802 | 1.0405   | 0.5203 |
| 12     | 0.9499   | 0.4750 | 1.1818   | 0.5909 | 1.4107   | 0.7054 | 1.2853   | 0.6427 | 1.0521   | 0.5261 |
| 13     | 0.9732   | 0.4866 | 1.2139   | 0.6070 | 1.4511   | 0.7256 | 1.3203   | 0.6601 | 1.0174   | 0.5087 |
| 14     | 0.7952   | 0.3976 | 0.7417   | 0.3709 | 0.7062   | 0.3531 | 0.8067   | 0.4034 | 0.9834   | 0.4917 |
| 15     | 0.7947   | 0.3974 | 0.7445   | 0.3723 | 0.7120   | 0.356  | 0.8970   | 0.4485 | 0.9254   | 0.4627 |

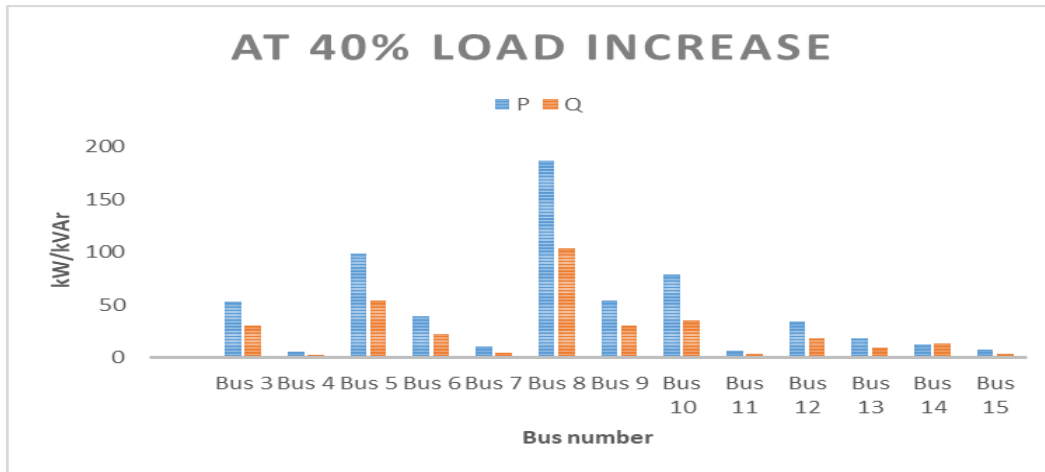


Figure 4.11: PQ load at 40% load increase without UPFC

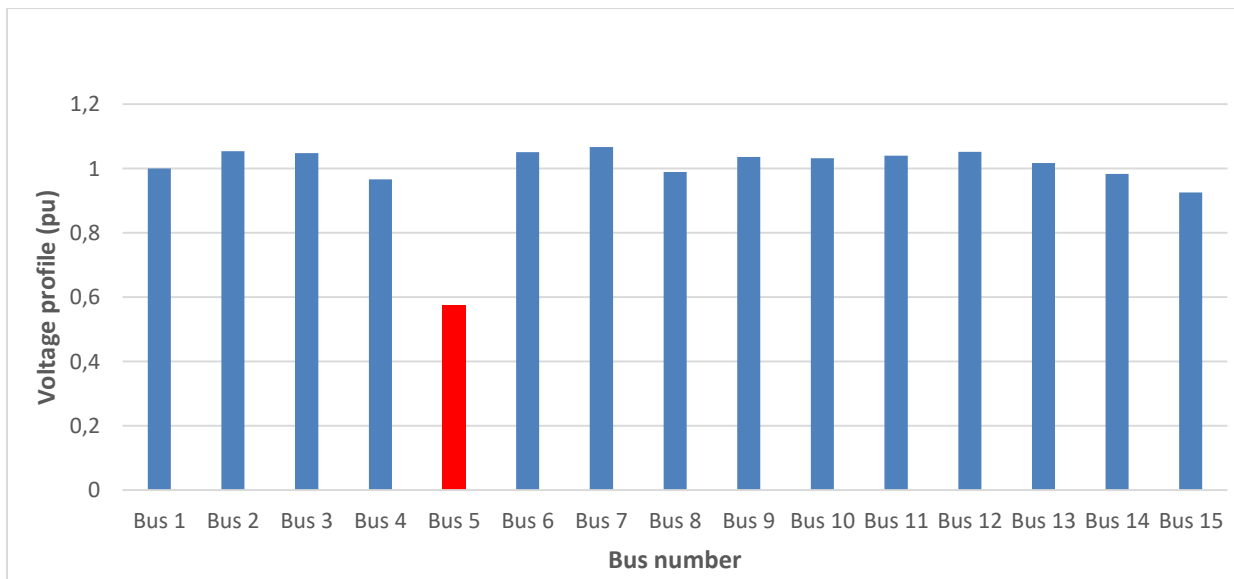


Figure 4.12: Voltage profile for all buses before UPFC placement at 40% load increase

By running the load flow, the output results from the calculations indicate the increment in power losses as PQ increases, at 40% load increase all buses are almost stable as it between 0.95-1.05 pu except bus 5. Fig.4.12 highlighting the bus 5 as a weakest bus due to its low voltage profile of 0.5 pu. As was mentioned from chapter 1 that the UPFC should be place at the weakest bus in order to improve the voltage profile and loss mitigation. As

bus 5 is the bus that is more stressed. Sense, is the bus that is most sensitive to a voltage instability. Therefore, the following chapter will be focusing on improving the voltage profile and minimising power losses. For power quality control as well as better usage of line capacity UPFC should be permanently installed at bus 5.

# CHAPTER FIVE

## PLACEMENT OF UPFC IN DISTRIBUTION NETWORK

### 5.1 Modelling of UPFC in *MATLAB*

#### 5.1.1 Description of a UPFC

The model of a UPFC shown in Fig.5.1 its specifications and parameters was taken from [68].

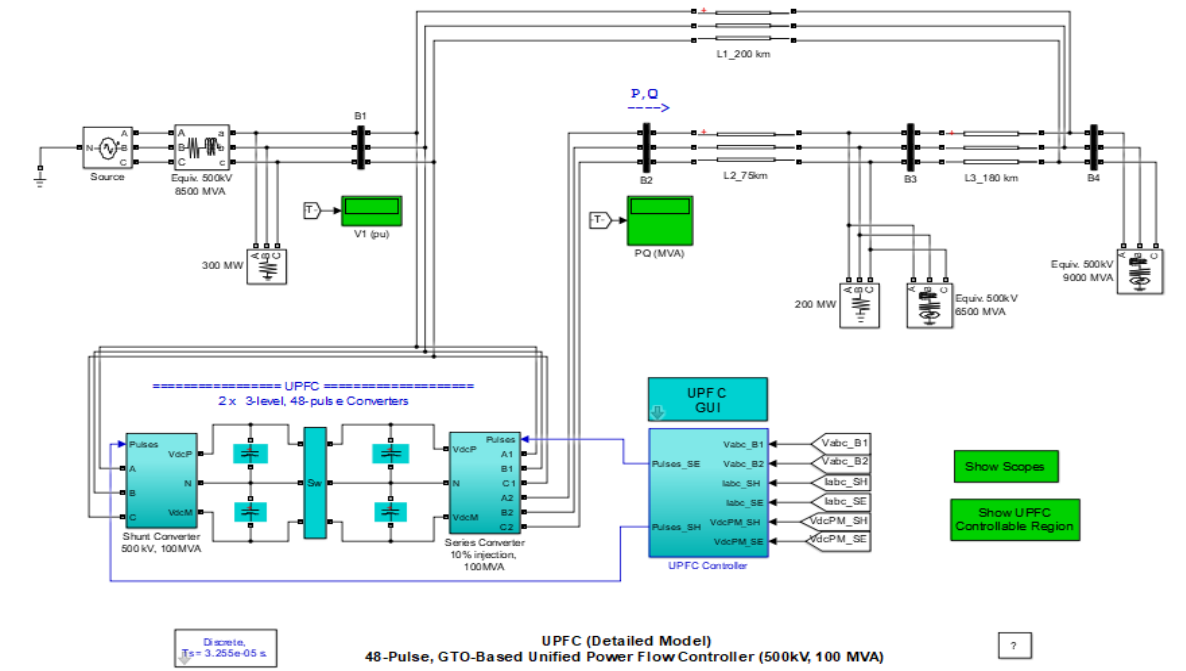


Figure 5.1: UPFC model system in *MATLAB*

The UPFC located at the left end of the 75-km line L2, between the 500 kV buses B1 and B2, is used to control the active and reactive powers flowing through bus B2 while controlling voltage at bus B1. It consists of two 100-MVA, three-level, 48-pulse GTO-based converters, one connected in shunt at bus B1 and the other is connected in series between buses B1 and B2. The shunt and series converters can exchange power through a DC bus. The series converter can inject a maximum of 1pu of the rated phase voltage in series with line L2. The VSCs of the UPFC can be operated in three modes:

- STATCOM when consider only shunt converter by disconnecting the switch

(b).SSSC when consider only series converter by disconnecting the switch

(c).UPFC when combining STATCOM and SSSC by closing the switch

The mode of operation as well as the reference voltage and reference power values can be changed by means of the "UPFC GUI" block.

### 5.1.2 Simulation and results

The simulation results of the UPFC is showing the increase of active and reactive power through monitored line, hence the UPFC simulation was run separated with the IEEE-15 bus system under study in order to evaluate the performance of UPFC before installing on the system under study.

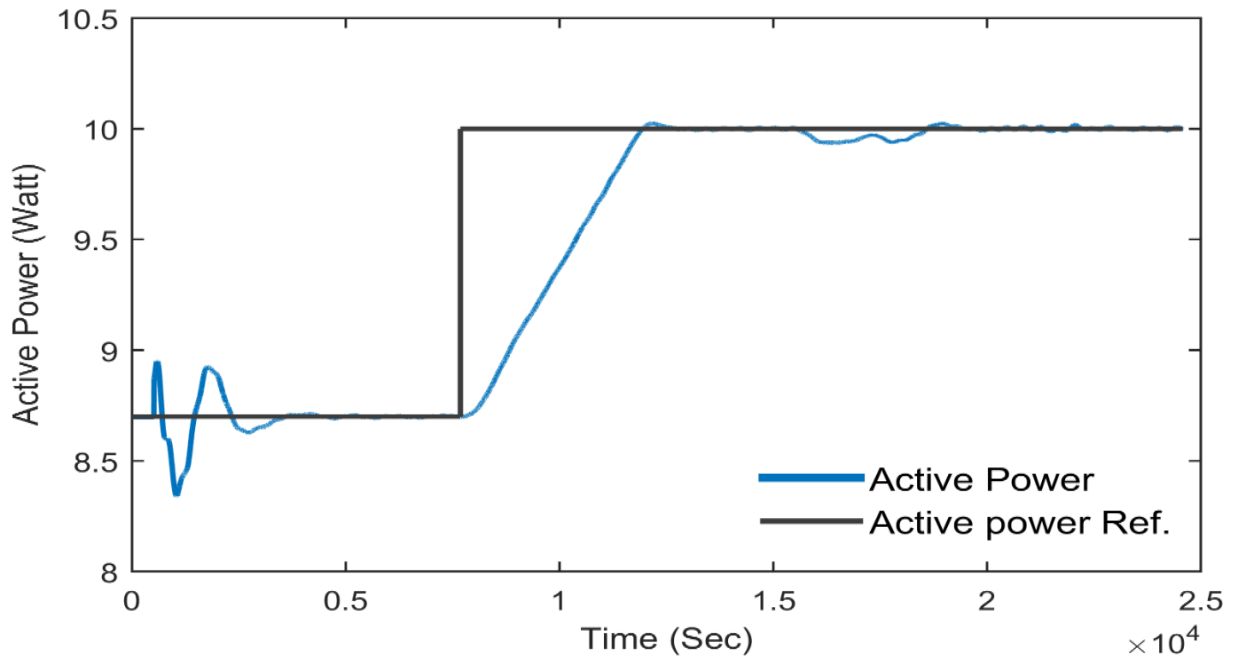


Figure 5.2: Active power response after UPFC placement

Concentrating on Fig.5.2, the simulation was run for 2.5 seconds, after the transient period the steady state was reached in 0.4 seconds and the reference has changed at 0.72 seconds and it is observed that the time taken by the UPFC to grow from 8.7pu (870MW) to 10pu (100MW) is from 0.79 to 1.3 seconds.

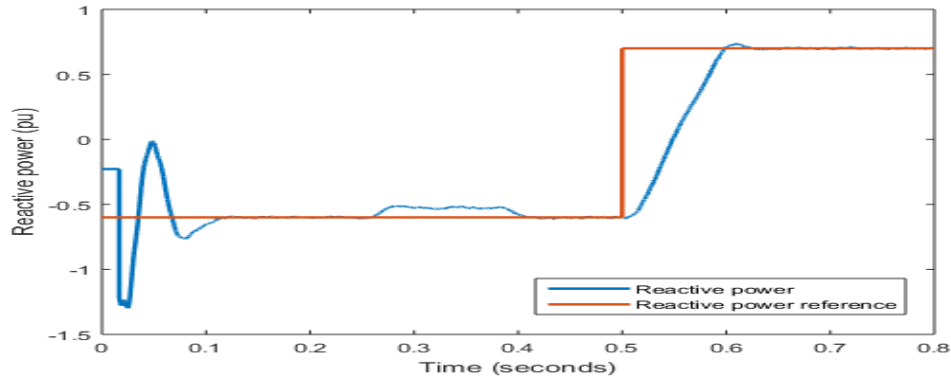


Figure 5.3: Reactive power response after UPFC placement

The Fig.5.3 showing the influence of the UPFC for reactive power flow which is conveyed through the line. The activeness of the UPFC was noticed at around 0.56 seconds and its take less than 0.1 second to grow reactive power from -0.6pu (-60MVar) increased to 0.7pu (70MVar). By comparing active and reactive power response, it is observed that reactive power is faster than the active power in terms of growing time.

### 5.1.3 Conclusion

This piece of simulation and investigation provide the possibility of installing the UPFC device on the IEEE-15 bus system under study. *MATLAB* software was used to conduct this investigation by simulating the interconnected system in Fig. 5.1. The impact and application of UPFC for controlling active and reactive power flow have been explored in this study. The simulation results demonstrate the usefulness of the UPFC as it indicating a fast operating time especially on reactive power of the line. Finally, UPFC is effective in treating dynamic system responses.

## 5.2 Placement of UPFC at bus 5

### 5.2.1 Load flow study with UPFC placement

The load data were exponentially increased in stairs steps of 10% up to 40% with and without UPFC placement. Simulation studies were done for different scenarios in IEEE-15 bus distribution feeder network. Five different scenarios are considered for the present study which are as follows:

- Scenario 1: The network is running on a normal load condition.
- Scenario 2: 10% load increase with and without UPFC.
- Scenario 3: 20% load increase with and without UPFC.
- Scenario 4: 30% load increase with and without UPFC.
- Scenario 5: 40% load increase with and without UPFC.

### 5.2.2 Overall analysis for voltage profile improvement

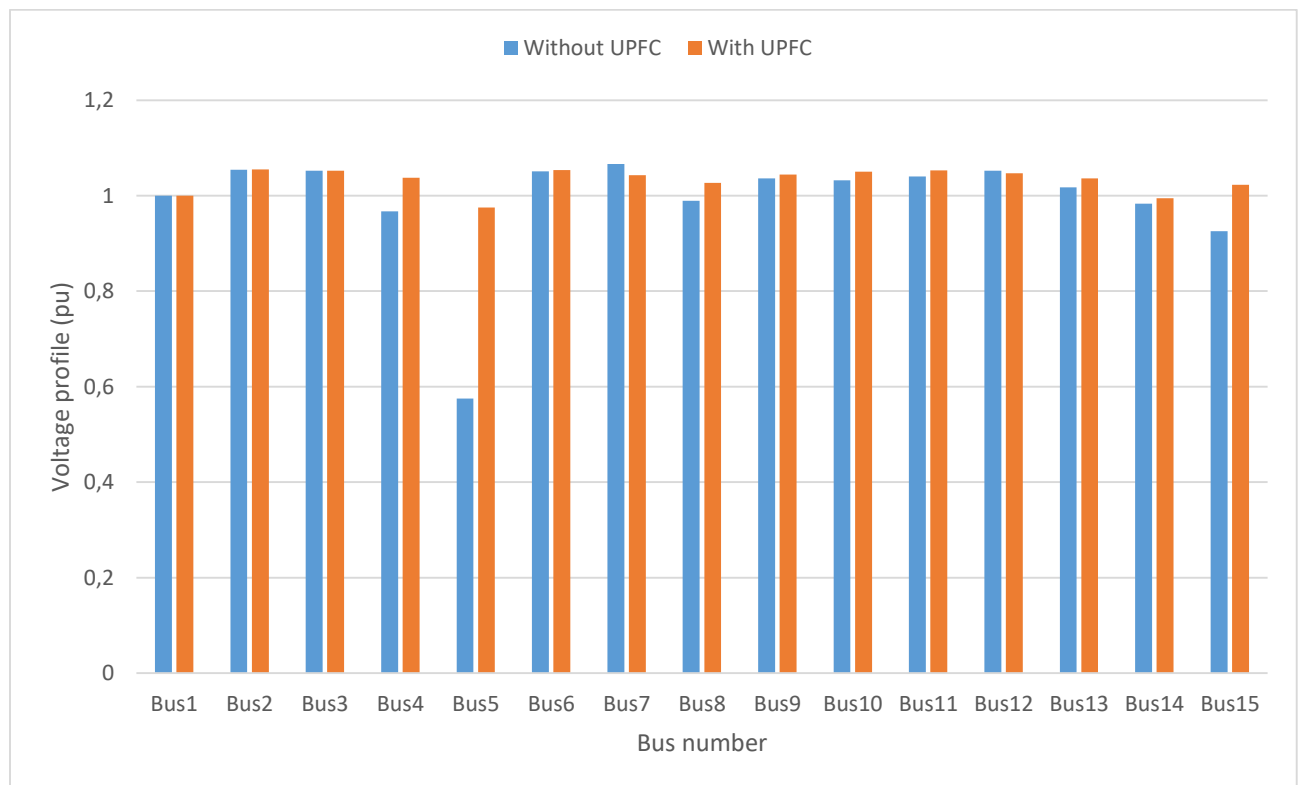


Figure 5.4: Comparison of voltage profile for all buses after UPFC placement at 40% load increase



Table 5.1: Comparison of voltage profile between before and after UPFC placement

| Bus No.      | With UPFC     | Without UPFC |
|--------------|---------------|--------------|
| Bus 1        | 1             | 1            |
| Bus 2        | 1.0551        | 1.0543       |
| Bus 3        | 1.0520        | 1.0486       |
| Bus 4        | 1.0374        | 0.9669       |
| <b>Bus 5</b> | <b>0,9750</b> | <b>0,5</b>   |
| Bus 6        | 1.0539        | 1.0512       |
| Bus 7        | 1.0429        | 1.0666       |
| Bus 8        | 1.0270        | 0.9895       |
| Bus 9        | 1.0443        | 1.0360       |
| Bus 10       | 1.05          | 1.0323       |
| Bus 11       | 1.0530        | 1.0405       |
| Bus 12       | 1.0472        | 1.0521       |
| Bus 13       | 1.0360        | 1.0174       |
| Bus 14       | 0.9943        | 0.9834       |
| Bus 15       | 1.0230        | 0.9254       |

### 5.2.3 Overall analysis for power losses reduction

Table 5.2: Displaying the total power losses with and without UPFC placement and its reduction

| Total power losses in IEEE-15 bus system |                          |                              |                                   |                                     |
|------------------------------------------|--------------------------|------------------------------|-----------------------------------|-------------------------------------|
|                                          | Active power losses (kW) | Reactive power losses (kVAr) | Active power losses reduction (%) | Reactive power losses reduction (%) |
| Without UPFC                             | 620                      | 90                           | 0                                 | 0                                   |
| With UPFC                                | 610                      | 330                          | 9,83%                             | 27,30%                              |

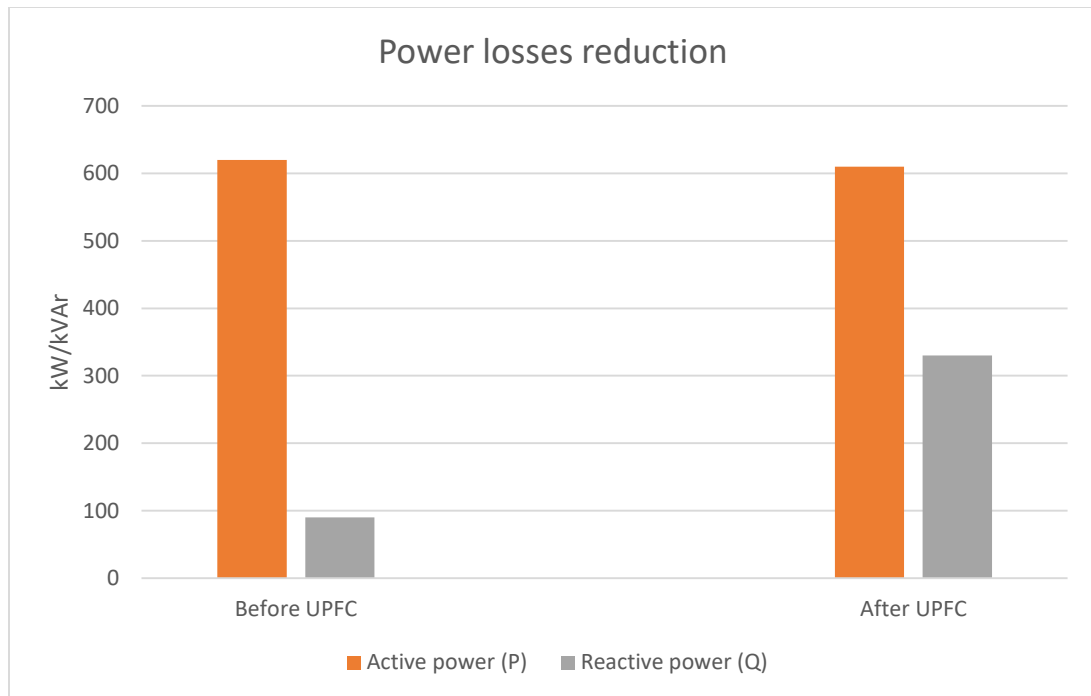


Figure 5.5: Active and reactive power losses reduction after UPFC placement

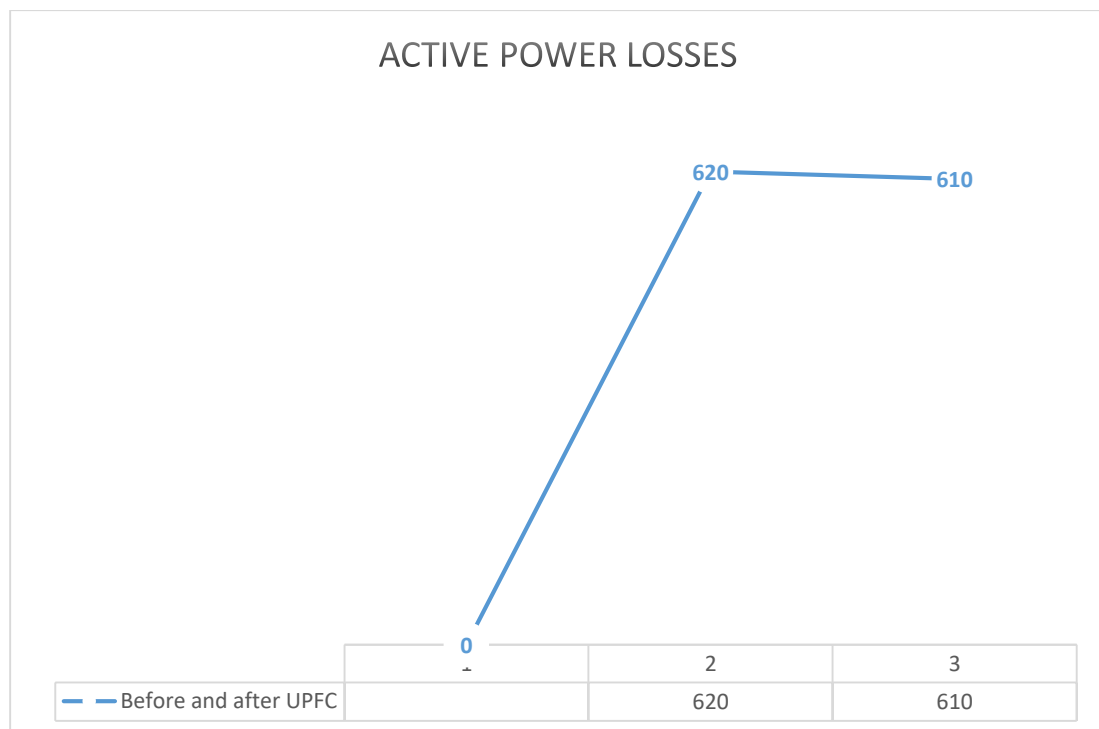


Figure 5.6: Comparison of active power losses before and after UPFC placement

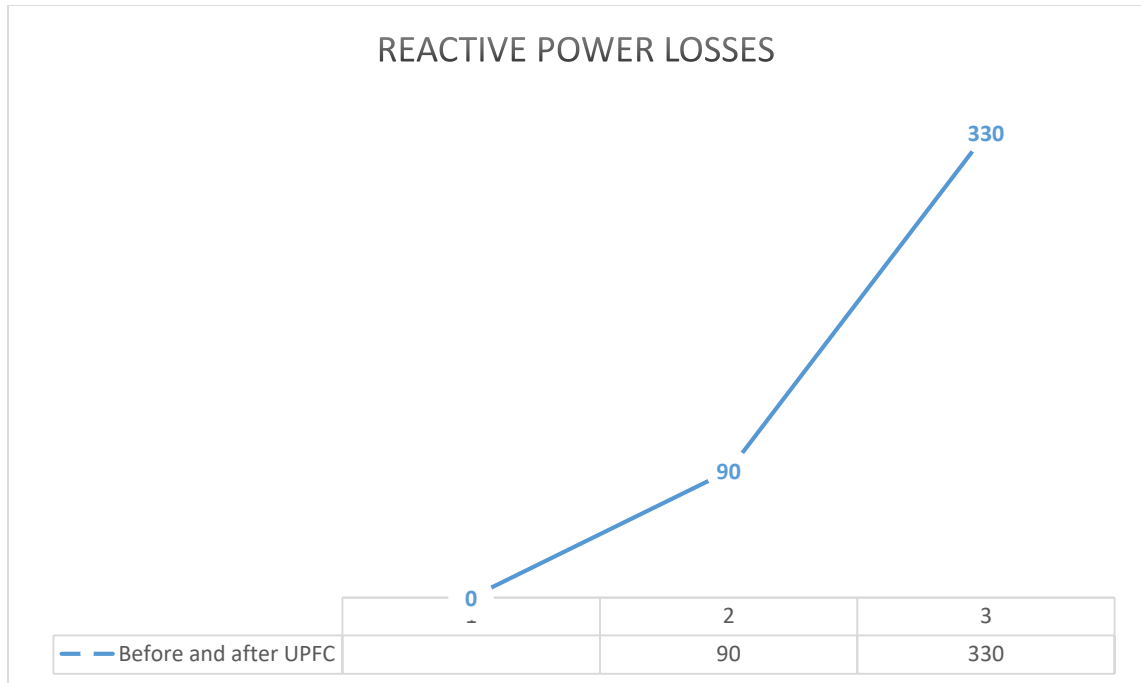


Figure 5.7: Comparison of reactive power losses before and after UPFC placement

### 5.3 Discussion

The real and reactive power plots with increase in system loading is given in Fig.4.5 for MW and MVar increase. The voltage profile of all busses is given in Fig.4.12 without considering the UPFC placement as well as it is also observe that when system loading is increase to 40% the bus 5 is highly affected in terms of voltage profile and may lead to the voltage instability of the complete network. Hence UPFC should be placed at this bus to improve the voltage profile of the DN. The UPFC has the ability to increase the voltage profile at the weakest bus and further results in power losses reduction simultaneously. Under the stress condition described in Fig.4.12, after UPFC placement at bus 5 the load flow was run again and the obtain results are listed in Table 5.1. The comparative analysis of voltage profile of IEEE 15 bus DN is shown in Fig.5.4 for 40% load increase with and without UPFC placement. It is observe that all busses voltages increase significantly after placing the UPFC on bus 5. At bus 5, the voltage has jump from 0.5750 p.u. to 0.9750 p.u. lead to the voltage stability of the network. Busses 11-13 are the strongest busses in terms of enhancement in voltage profile of this network. Further, the graphical analysis of Bus 5 is also carried out in terms of real and reactive power improvement and it is evident

from the results of Fig.4.12 that there is an significant decrement in real power loses of the network which reduces from 620kW to 610kW and reactive power from 90kVAr to 330kVAr and this is an significant enhancement with respect to voltage stability and network losses reduction.

## CHAPTER SIX

### CONCLUSION AND RECOMMENDATIONS

#### 6.1 Conclusion and recommendations

The present research work shows an enhance performance of a UPFC and its future promising technology to improve the voltage profile and power loses mitigation for DN. The feasibility studies of UPFC is tested on standard IEEE-15 bus test system.

The investigation was carried out using standard *MATLAB* software. The system was firstly simulated by running a load flow tool with Newton-Raphson method in order to observe the bus voltage magnitude, the power that is being generated, power that is consumed, and the power that is lost (power loses) through the network.

The weakest bus was determined at the 40% increase in system loading and may lead to the voltage instability of the system. However, after UPFC placement there is an significant enhancement of voltages of all busses as well as Bus 5 voltage jump from 0.5750 to 0.9750 p.u. and shifting the bus 5 from voltage instability to stable zone. It is also observe that the active and reactive power loses were decreased by 9.83% and 27.27% that fulfil the beauty of the UPFC installation in the DNs further it also shows promise to mitigate the voltage instability problem of the modern DNs.

These different aspects give scope for the future research work as P-Q load increases up to 40%. Incidentally, P-Q load is almost balanced in residential areas but in industrials Q is very high,

- a) hence in future research work the Q load will be increased separately and observe the results.
- b) Investigation of FACTS Devices Capabilities in Voltage Stability of DN, this project research work aims to investigate the capability of

UPFC in controlling voltage in DN with high penetration of Renewable Energy Sources (RES).

- c) Analysis and Comparing the performance of Voltage Stability Indices, these indices will be tested in different networks such as; small 5-bus system network and in a larger 15-bus system. the performance comparison will be based on three characteristics: their accuracy, robustness to uncertainty and usable for control purposes.

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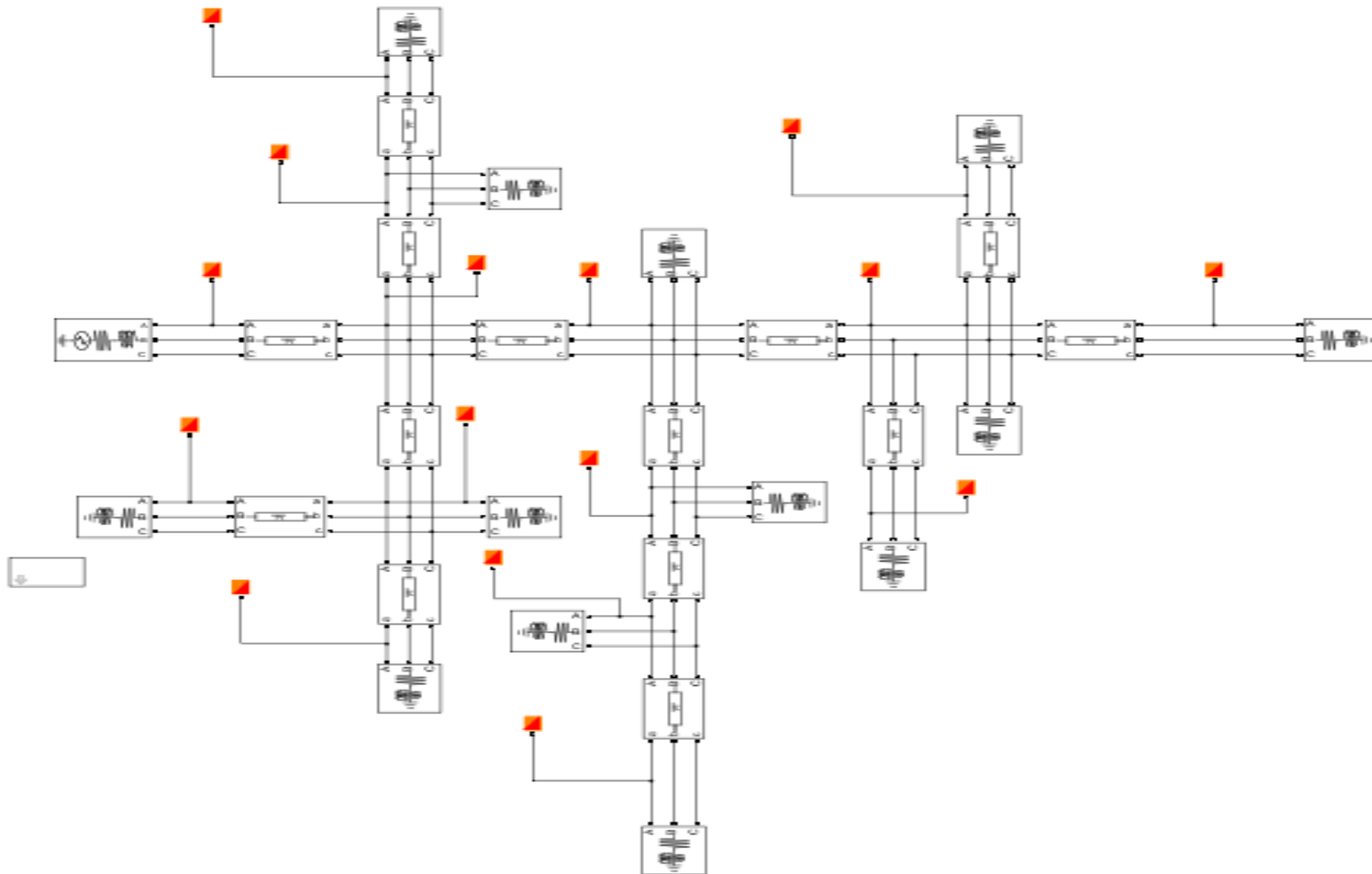
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## APPENDICES

### Appendix A: IEEE-15 bus on the test system without UPFC placement



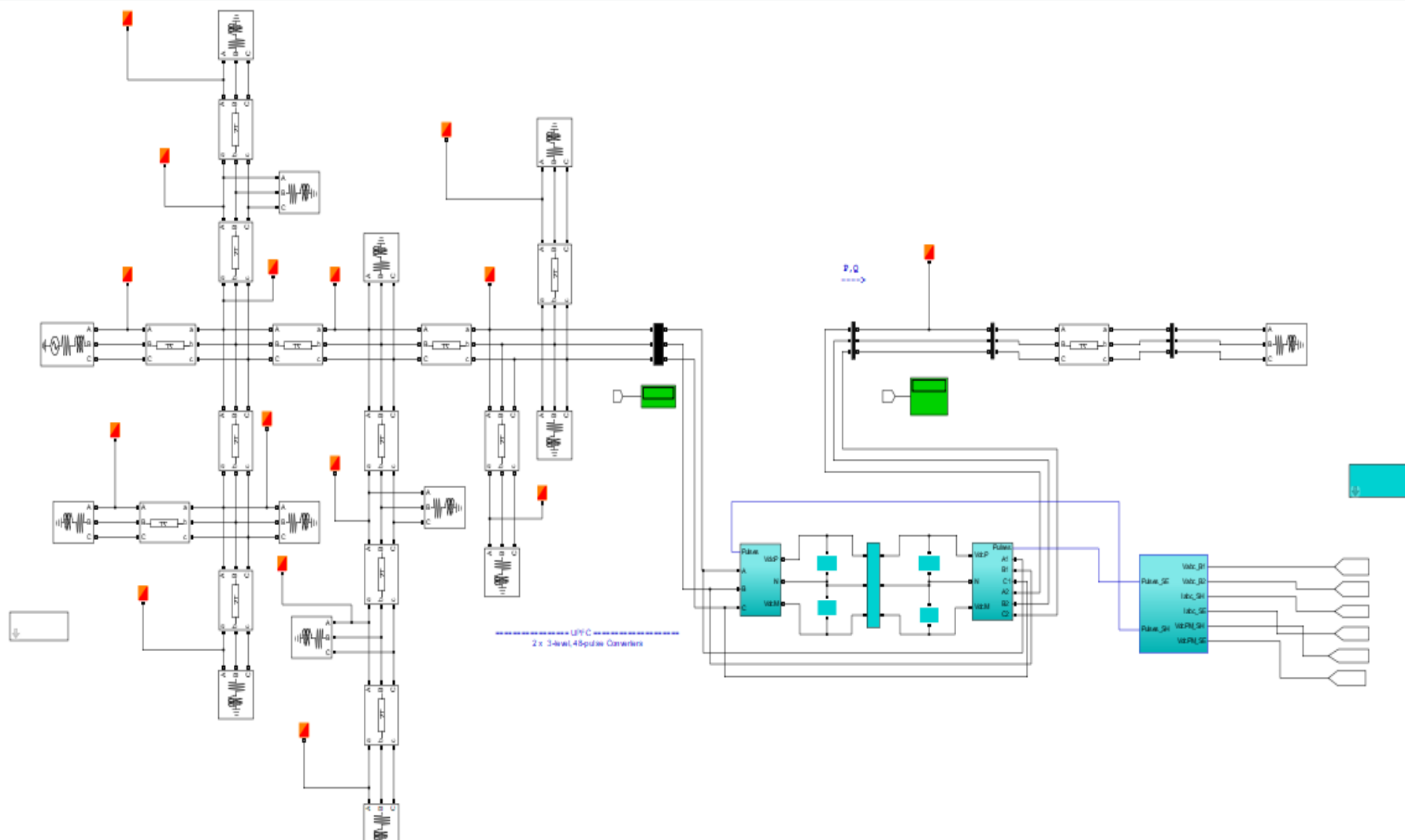
**Table A1: Line data for IEEE-15 bus system**

| From bus | To bus | R(ohms) | X(ohms) | B/2(mho) |
|----------|--------|---------|---------|----------|
| 1        | 2      | 0.0005  | j0.0012 | j0.6987  |
| 2        | 3      | 0.0304  | j0.0355 | j0.75    |
| 3        | 4      | 0.0015  | j0.0036 | j0.2572  |
| 4        | 5      | 0.0005  | j0.0012 | j0.146   |
| 2        | 9      | 0.0251  | j0.0294 | j0.2214  |
| 9        | 10     | 0.366   | j0.1864 | j0.2138  |
| 2        | 6      | 0.3811  | j0.1941 | j0.1342  |
| 6        | 7      | 0.0922  | j0.047  | j0.0434  |
| 6        | 8      | 0.0493  | j0.0251 | j0.1476  |
| 3        | 11     | 0.819   | j0.2707 | j0.113   |
| 11       | 12     | 0.1872  | j0.0619 | j0.1389  |
| 12       | 13     | 0.7114  | j0.2351 | j0.078   |
| 4        | 14     | 1.03    | j0.34   | j0.3804  |
| 4        | 15     | 1.044   | j0.345  | j0.0729  |

**Table A2: Load data for IEEE-15 bus system**

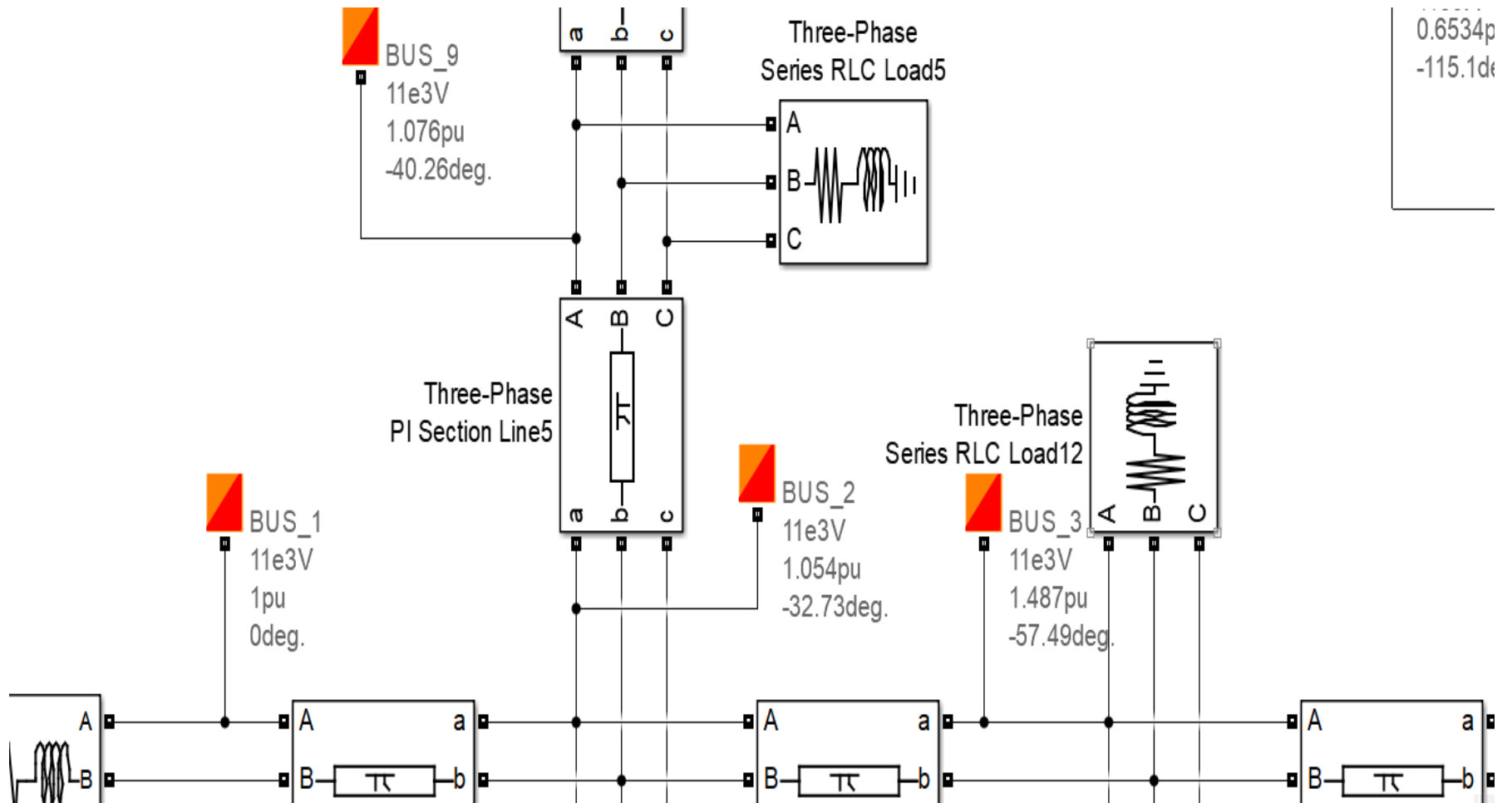
| Normal load |                 |                       |
|-------------|-----------------|-----------------------|
| Bus No      | Real power (kW) | Reactive power (kVAr) |
| 3           | 37.233          | 21                    |
| 4           | 4.067           | 1.54                  |
| 5           | 69.3            | 37.8                  |
| 6           | 27.72           | 15.4                  |
| 7           | 7.392           | 3.5                   |
| 8           | 131.04          | 72.8                  |
| 9           | 38.22           | 21                    |
| 10          | 55.44           | 24.5                  |
| 11          | 4.62            | 2.45                  |
| 12          | 24.024          | 12.985                |
| 13          | 12.936          | 7                     |
| 14          | 8.778           | 9.8                   |
| 15          | 5.544           | 2.8                   |

## Appendix B: IEEE-15 bus on the test system with UPFC placement





## Appendix B1: IEEE-15 bus on the test system grid labelling



## Appendix C: load flow results

| Frequency (Hz): 60.0 Base power (VA): 1e+05 Max iterations: 50 F |             |          |        |            |           |              |        |          |             |             |           |                 |           |             |
|------------------------------------------------------------------|-------------|----------|--------|------------|-----------|--------------|--------|----------|-------------|-------------|-----------|-----------------|-----------|-------------|
|                                                                  | Block type  | Bus type | Bus ID | Vbase (kV) | Vref (pu) | Vangle (deg) | P (MW) | Q (Mv... | Qmin (Mvar) | Qmax (Mvar) | V_LF (pu) | Vangle_LF (deg) | P_LF (MW) | Q_LF (Mvar) |
| 1                                                                | Vsrc        | swing    | BUS_1  | 11.00      | 1         | 0.00         | 0.00   | 0.00     | -Inf        | Inf         | 1         | 0.00            | 0.62      | 0.09        |
| 2                                                                | Bus         | -        | BUS_2  | 11.00      | 1         | 0.00         | 0.00   | 0.00     | 0.00        | 0.00        | 1.0543    | -32.73          | 0.00      | 0.00        |
| 3                                                                | RLC load PQ |          | BUS_13 | 11.00      | 1         | 0.00         | 0.02   | 0.01     | -Inf        | Inf         | 2.0140    | -60.47          | 0.02      | 0.01        |
| 4                                                                | RLC load PQ |          | BUS_12 | 11.00      | 1         | 0.00         | 0.03   | 0.02     | -Inf        | Inf         | 1.9544    | -60.15          | 0.03      | 0.02        |
| 5                                                                | RLC load PQ |          | BUS_11 | 11.00      | 1         | 0.00         | 0.01   | 0.00     | -Inf        | Inf         | 1.7405    | -58.89          | 0.01      | 0.00        |
| 6                                                                | RLC load PQ |          | BUS_15 | 11.00      | 1         | 0.00         | 0.01   | 0.00     | -Inf        | Inf         | 0.6654    | -113.68         | 0.01      | 0.00        |
| 7                                                                | RLC load PQ |          | BUS_14 | 11.00      | 1         | 0.00         | 0.01   | 0.01     | -Inf        | Inf         | 0.6534    | -115.06         | 0.01      | 0.01        |
| 8                                                                | RLC load PQ |          | BUS_3  | 11.00      | 1         | 0.00         | 0.05   | 0.03     | -Inf        | Inf         | 1.4869    | -57.49          | 0.05      | 0.03        |
| 9                                                                | RLC load PQ |          | BUS_4  | 11.00      | 1         | 0.00         | 0.01   | 0.00     | -Inf        | Inf         | 0.6569    | -113.00         | 0.01      | 0.00        |
| 10                                                               | RLC load PQ |          | BUS_5  | 11.00      | 1         | 0.00         | 0.10   | 0.05     | -Inf        | Inf         | 0.5750    | -125.56         | 0.10      | 0.05        |
| 11                                                               | RLC load PQ |          | BUS_6  | 11.00      | 1         | 0.00         | 0.04   | 0.02     | -Inf        | Inf         | 1.0512    | -34.48          | 0.04      | 0.02        |
| 12                                                               | RLC load PQ |          | BUS_7  | 11.00      | 1         | 0.00         | 0.01   | 0.01     | -Inf        | Inf         | 1.0666    | -34.82          | 0.01      | 0.01        |
| 13                                                               | RLC load PQ |          | BUS_8  | 11.00      | 1         | 0.00         | 0.19   | 0.10     | -Inf        | Inf         | 0.9895    | -41.48          | 0.19      | 0.10        |
| 14                                                               | RLC load PQ |          | BUS_9  | 11.00      | 1         | 0.00         | 0.05   | 0.03     | -Inf        | Inf         | 1.0760    | -40.26          | 0.05      | 0.03        |
| 15                                                               | RLC load PQ |          | BUS_10 | 11.00      | 1         | 0.00         | 0.08   | 0.04     | -Inf        | Inf         | 1.0717    | -43.91          | 0.08      | 0.04        |

## Appendix D: load flow results: Grid summary

The Load Flow converged in 5 iterations !

SUMMARY for subnetwork No 1

|                   |   |    |          |    |            |
|-------------------|---|----|----------|----|------------|
| Total generation  | : | P= | 0.62 MW  | Q= | 0.09 Mvar  |
| Total PQ load     | : | P= | 0.61 MW  | Q= | 0.33 Mvar  |
| Total Zshunt load | : | P= | -0.00 MW | Q= | 0.00 Mvar  |
| Total ASM load    | : | P= | 0.00 MW  | Q= | 0.00 Mvar  |
| Total losses      | : | P= | 0.01 MW  | Q= | -0.25 Mvar |

1 : BUS\_1 V= 1.000 pu/11kV 0.00 deg ; Swing bus  
Generation : P= 0.62 MW Q= 0.09 Mvar  
PQ\_load : P= 0.00 MW Q= 0.00 Mvar  
Z\_shunt : P= -0.00 MW Q= -0.00 Mvar  
--> BUS\_2 : P= 0.62 MW Q= 0.09 Mvar

2 : BUS\_10 V= 1.072 pu/11kV -43.91 deg  
Generation : P= 0.00 MW Q= 0.00 Mvar  
PQ\_load : P= 0.08 MW Q= 0.03 Mvar  
Z\_shunt : P= 0.00 MW Q= 0.00 Mvar  
--> BUS\_9 : P= -0.08 MW Q= -0.03 Mvar

3 : BUS\_11 V= 1.741 pu/11kV -58.89 deg  
Generation : P= 0.00 MW Q= 0.00 Mvar  
PQ\_load : P= 0.01 MW Q= 0.00 Mvar  
Z\_shunt : P= 0.00 MW Q= -0.00 Mvar  
--> BUS\_12 : P= 0.05 MW Q= -0.36 Mvar  
--> BUS\_3 : P= -0.06 MW Q= 0.36 Mvar

4 : BUS\_12 V= 1.954 pu/11kV -60.15 deg  
Generation : P= 0.00 MW Q= 0.00 Mvar  
PQ\_load : P= 0.03 MW Q= 0.02 Mvar  
Z\_shunt : P= 0.00 MW Q= 0.00 Mvar  
--> BUS\_11 : P= -0.05 MW Q= 0.20 Mvar  
--> BUS\_13 : P= 0.02 MW Q= -0.22 Mvar

5 : BUS\_13 V= 2.014 pu/11kV -60.47 deg  
Generation : P= 0.00 MW Q= 0.00 Mvar  
PQ\_load : P= 0.02 MW Q= 0.01 Mvar  
Z\_shunt : P= 0.00 MW Q= -0.00 Mvar  
--> BUS\_12 : P= -0.02 MW Q= -0.01 Mvar

6 : BUS\_14 V= 0.653 pu/11kV -115.06 deg  
Generation : P= 0.00 MW Q= 0.00 Mvar  
PQ\_load : P= 0.01 MW Q= 0.01 Mvar  
Z\_shunt : P= 0.00 MW Q= 0.00 Mvar

```

--> BUS_4      : P=   -0.01 MW Q=   -0.01 Mvar

7 : BUS_15  V= 0.665 pu/11kV -113.68 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.01 MW Q=    0.00 Mvar
    Z_shunt    : P=    0.00 MW Q=    0.00 Mvar
--> BUS_4      : P=   -0.01 MW Q=   -0.00 Mvar

8 : BUS_2   V= 1.054 pu/11kV -32.73 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=   -0.00 MW Q=   -0.00 Mvar
    Z_shunt    : P=   -0.00 MW Q=    0.00 Mvar
--> BUS_1      : P=   -0.61 MW Q=    0.22 Mvar
--> BUS_3      : P=    0.24 MW Q=   -0.15 Mvar
--> BUS_6      : P=    0.24 MW Q=   -0.02 Mvar
--> BUS_9      : P=    0.13 MW Q=   -0.05 Mvar

9 : BUS_3   V= 1.487 pu/11kV -57.49 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.05 MW Q=    0.03 Mvar
    Z_shunt    : P=    0.00 MW Q=   -0.00 Mvar
--> BUS_11     : P=    0.06 MW Q=   -0.45 Mvar
--> BUS_2      : P=   -0.24 MW Q=    0.22 Mvar
--> BUS_4      : P=    0.13 MW Q=    0.19 Mvar

10 : BUS_4  V= 0.657 pu/11kV -113.00 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.01 MW Q=    0.00 Mvar
    Z_shunt    : P=    0.00 MW Q=    0.00 Mvar
--> BUS_14     : P=    0.01 MW Q=   -0.01 Mvar
--> BUS_15     : P=    0.01 MW Q=   -0.02 Mvar
--> BUS_3      : P=   -0.13 MW Q=   -0.03 Mvar
--> BUS_5      : P=    0.10 MW Q=    0.06 Mvar

11 : BUS_5  V= 0.575 pu/11kV -125.56 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.10 MW Q=    0.05 Mvar
    Z_shunt    : P=    0.00 MW Q=    0.00 Mvar
--> BUS_4      : P=   -0.10 MW Q=   -0.05 Mvar

12 : BUS_6  V= 1.051 pu/11kV -34.48 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.04 MW Q=    0.02 Mvar
    Z_shunt    : P=   -0.00 MW Q=    0.00 Mvar
--> BUS_2      : P=   -0.24 MW Q=   -0.03 Mvar
--> BUS_7      : P=    0.01 MW Q=   -0.06 Mvar
--> BUS_8      : P=    0.19 MW Q=    0.07 Mvar

13 : BUS_7  V= 1.067 pu/11kV -34.82 deg
    Generation : P=    0.00 MW Q=    0.00 Mvar
    PQ_load    : P=    0.01 MW Q=    0.01 Mvar
    Z_shunt    : P=   -0.00 MW Q=    0.00 Mvar
--> BUS_6      : P=   -0.01 MW Q=   -0.01 Mvar

14 : BUS_8  V= 0.990 pu/11kV -41.48 deg

```

```

        Generation : P=    0.00 MW Q=    0.00 Mvar
        PQ_load    : P=    0.19 MW Q=    0.10 Mvar
        Z_shunt    : P=   -0.00 MW Q=    0.00 Mvar
-->  BUS_6        : P=   -0.19 MW Q=   -0.10 Mvar

15 : BUS_9  V= 1.076 pu/11kV -40.26 deg
        Generation : P=    0.00 MW Q=    0.00 Mvar
        PQ_load    : P=    0.05 MW Q=    0.03 Mvar
        Z_shunt    : P=   -0.00 MW Q=    0.00 Mvar
-->  BUS_10       : P=    0.08 MW Q=   -0.03 Mvar
-->  BUS_2        : P=   -0.13 MW Q=   -0.00 Mvar

```